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SESSION 3

Ultra-High-Speed Transceivers

A 25Gb/s ADC-Based Serial Line Receiver in 32nm CMOS SOI

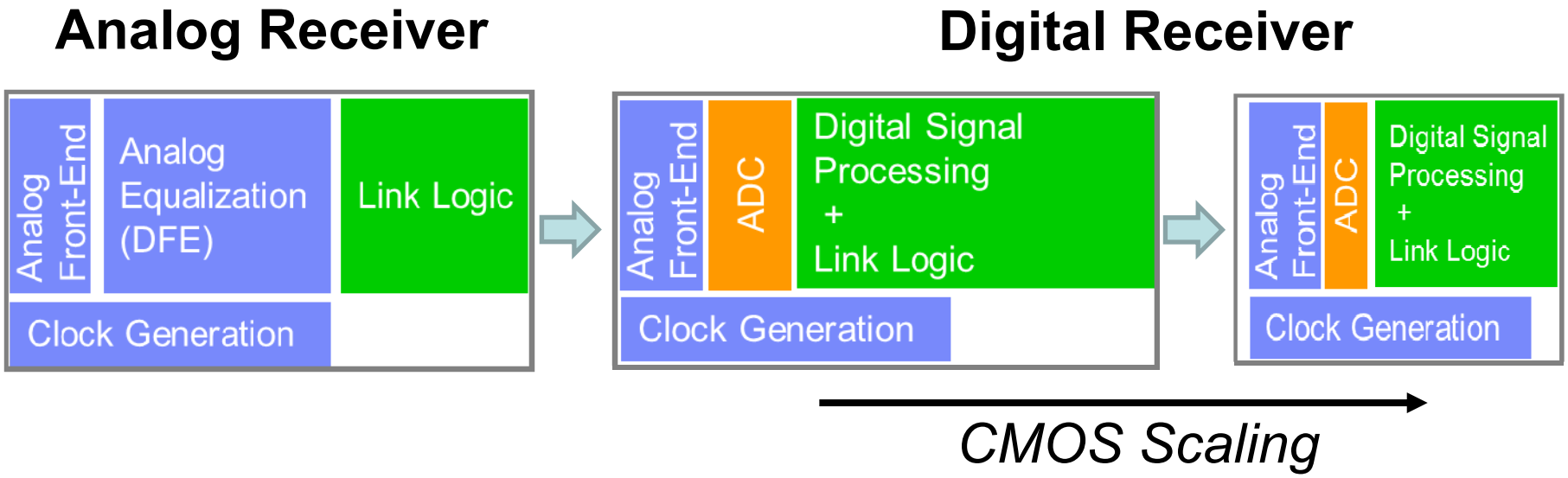
Sergey Rylov[1], Troy Beukema[1], Zeynep Toprak-Deniz[1], Thomas Toifl[2], Yong Liu[1], Ankur Agrawal[1], Peter Buchmann[2], Alexander Rylyakov[1], Michael Beakes[1], Benjamin Parker[1], Mounir Meghelli[1]

[1]IBM T. J. Watson Research Center
[2]IBM Zurich Research Laboratory

Outline

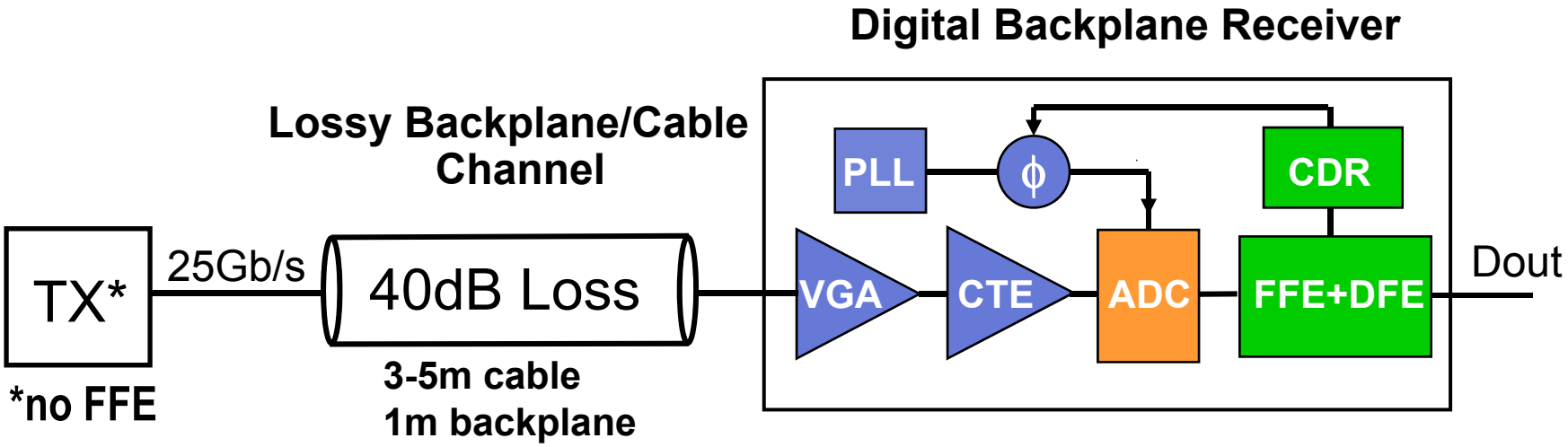
- Motivation
- Digital receiver architecture
- ADC implementation
- Digital blocks
- Experimental results
- Conclusion

Motivation for Digital Receiver



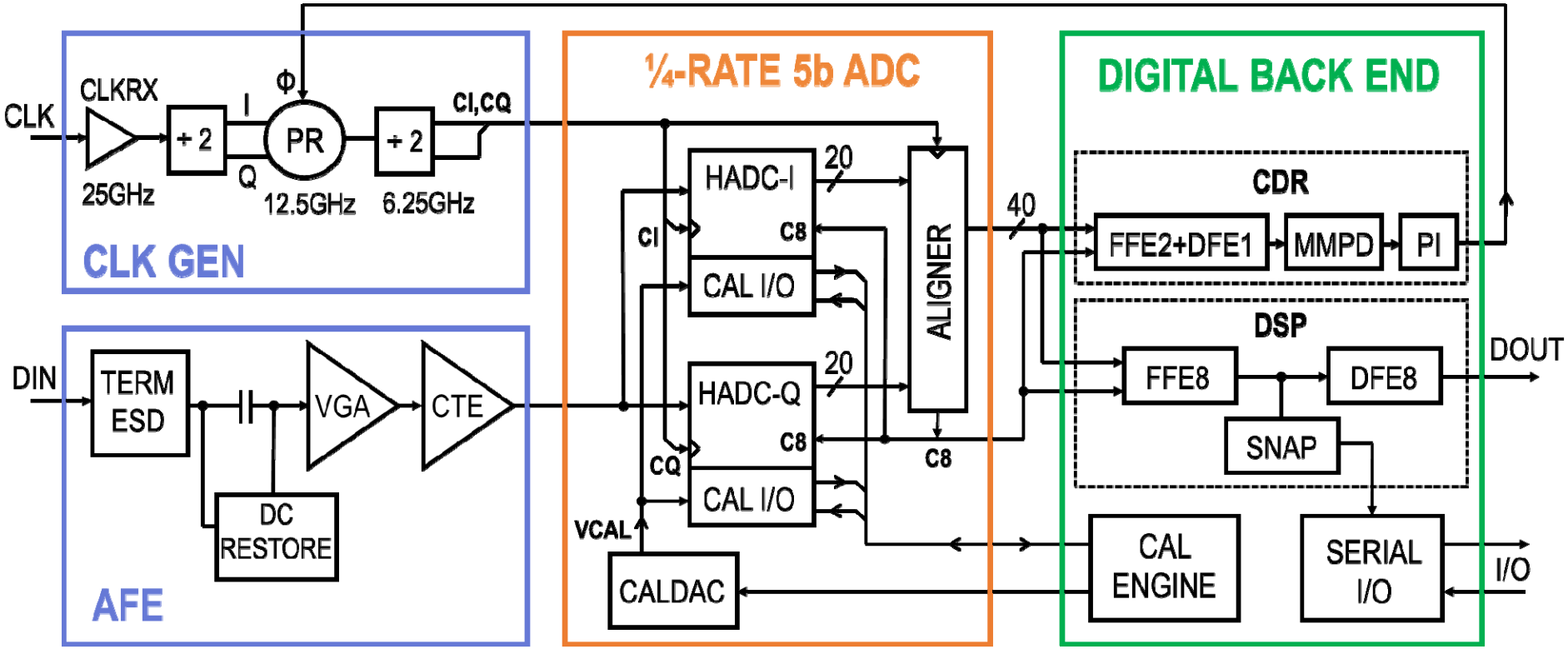
- Digital receivers leverage power/area reduction in advanced CMOS nodes better than analog designs
- Digital receivers are capable of supporting advanced line modulations needed as line data rates continue to scale to 56Gb/s and beyond

Digital Receiver Application



- Digital receiver performs all line equalization with no need for equalization in the transmitter
- 40+ dB end-to-end channel loss is expected at 25Gb/s in reflective, lossy backplane channels

Digital Receiver Architecture



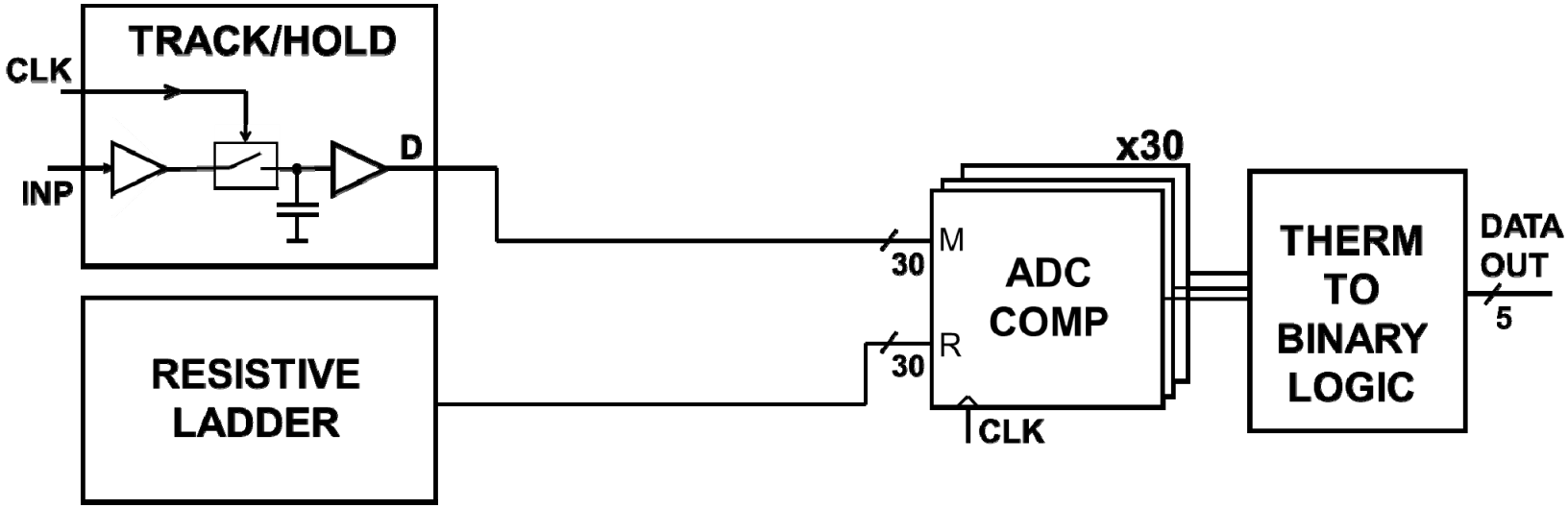
- ADC: self-calibrating quarter-rate 25GS/s 5 bit flash
- AFE and clock generation: re-use of 28GS/s HSS analog Rx
- Digital block: 8-tap FFE, 8-tap DFE, baud-rate CDR

Why Flash ADC

- Offers reasonable complexity, power, area at 5 bit resolution (sufficient for NRZ signaling)
- Very good scalability with technology node
- Easy to achieve metastability resistance
- Possible to achieve dynamic ADC calibration with low hardware overhead

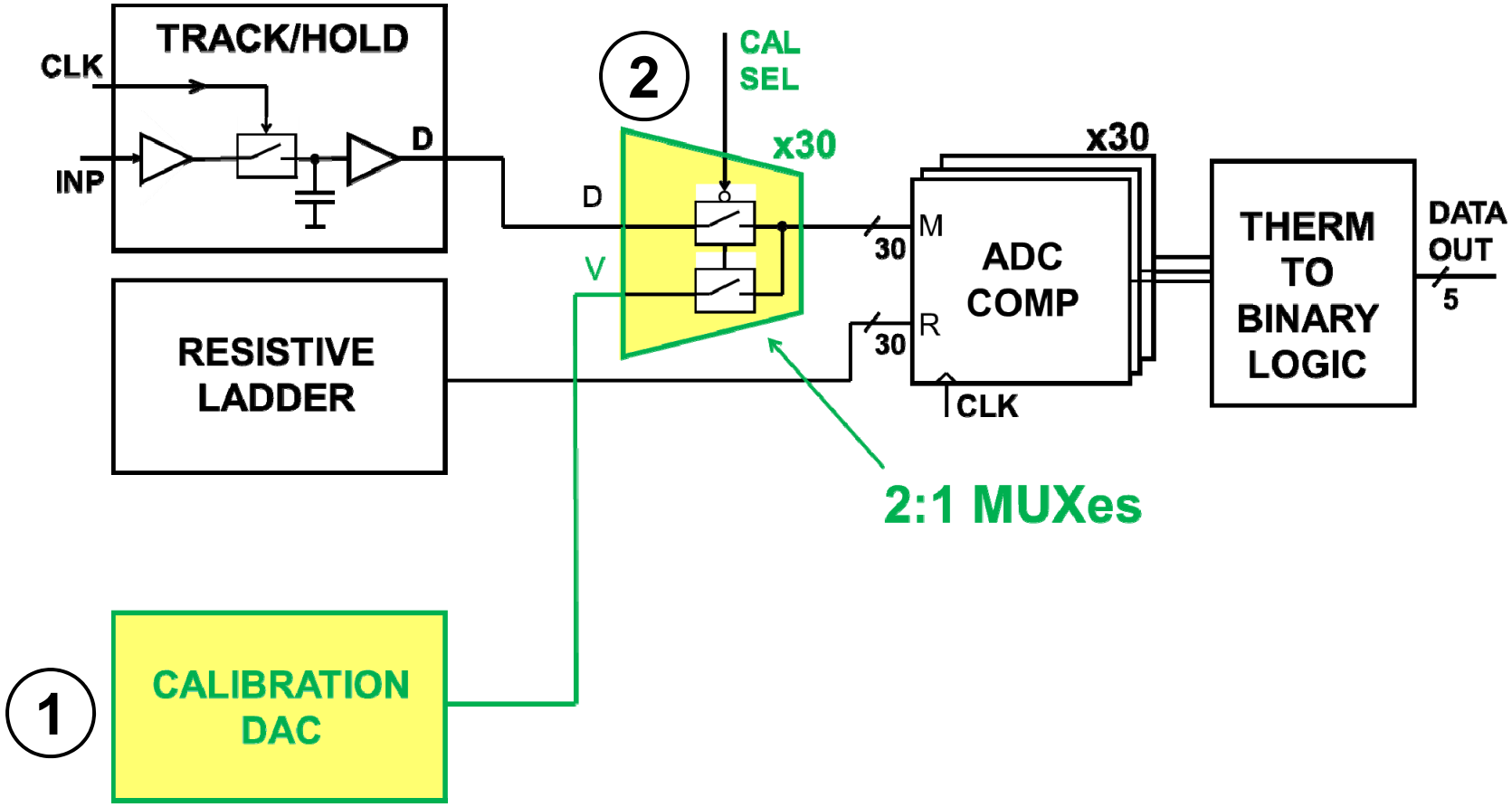
Overall flash ADC meets the system requirements of a Gigabit digital wireline receiver

ADC Self Calibration: Introduction



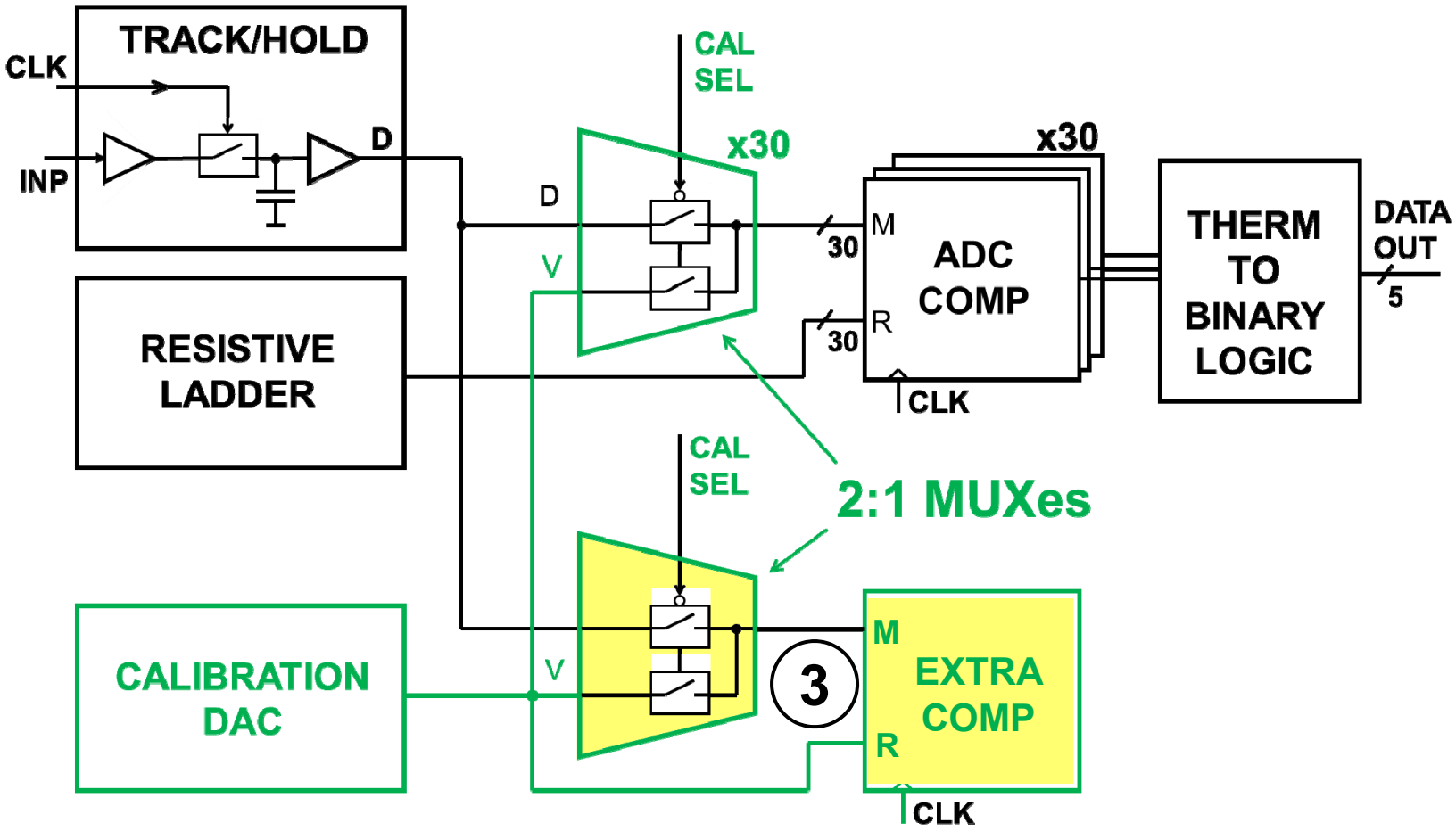
- Dynamic ADC calibration is a system requirement for a continuously operating link
- One can implement it in a flash ADC by adding <u>four</u> extra components

Self Calibration: Adding CALDAC+MUXes



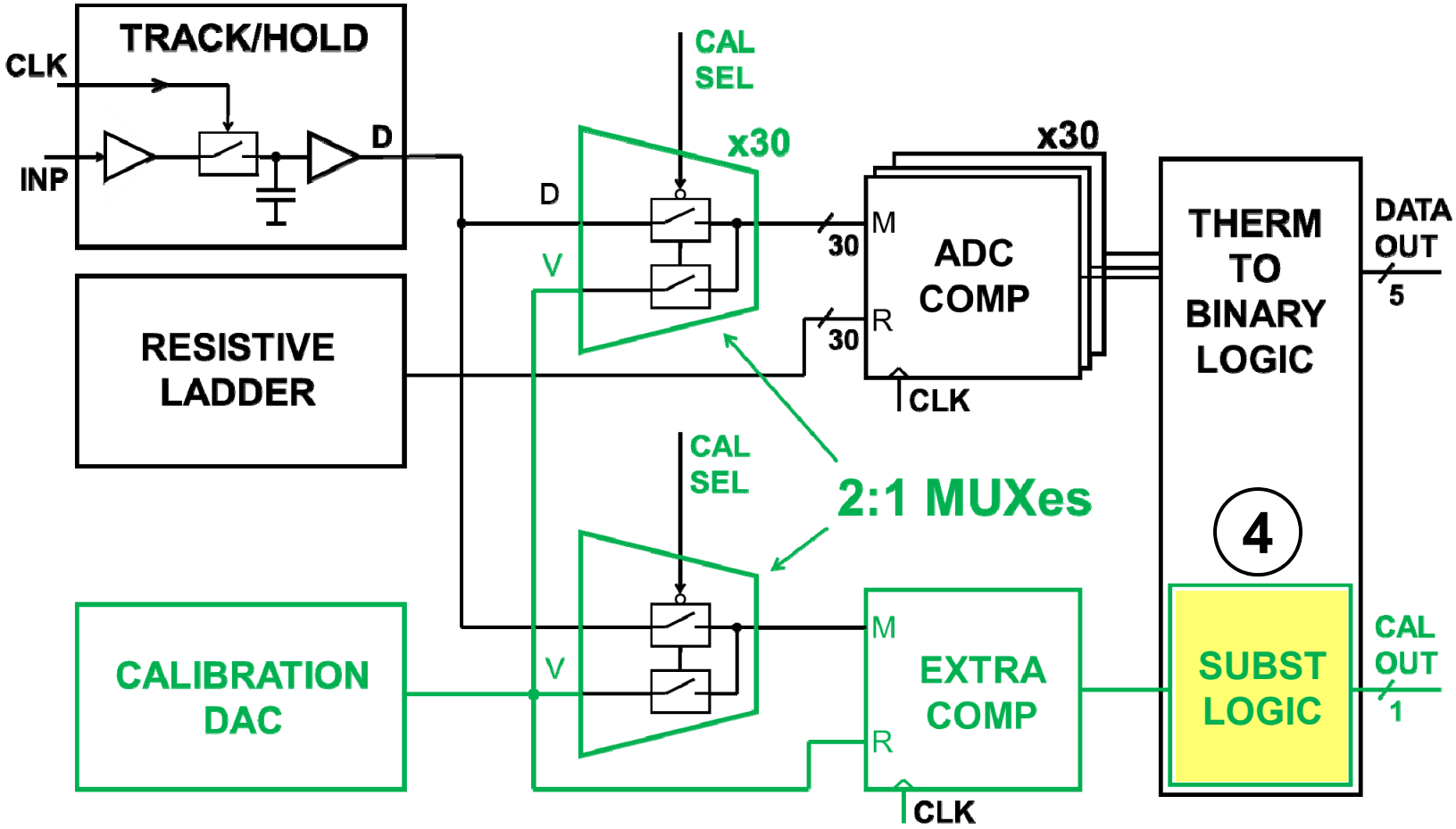
1. Add high precision Calibration DAC
2. Add 2:1 MUX at input of every comparator

Self Calibration: Adding Extra Comparator



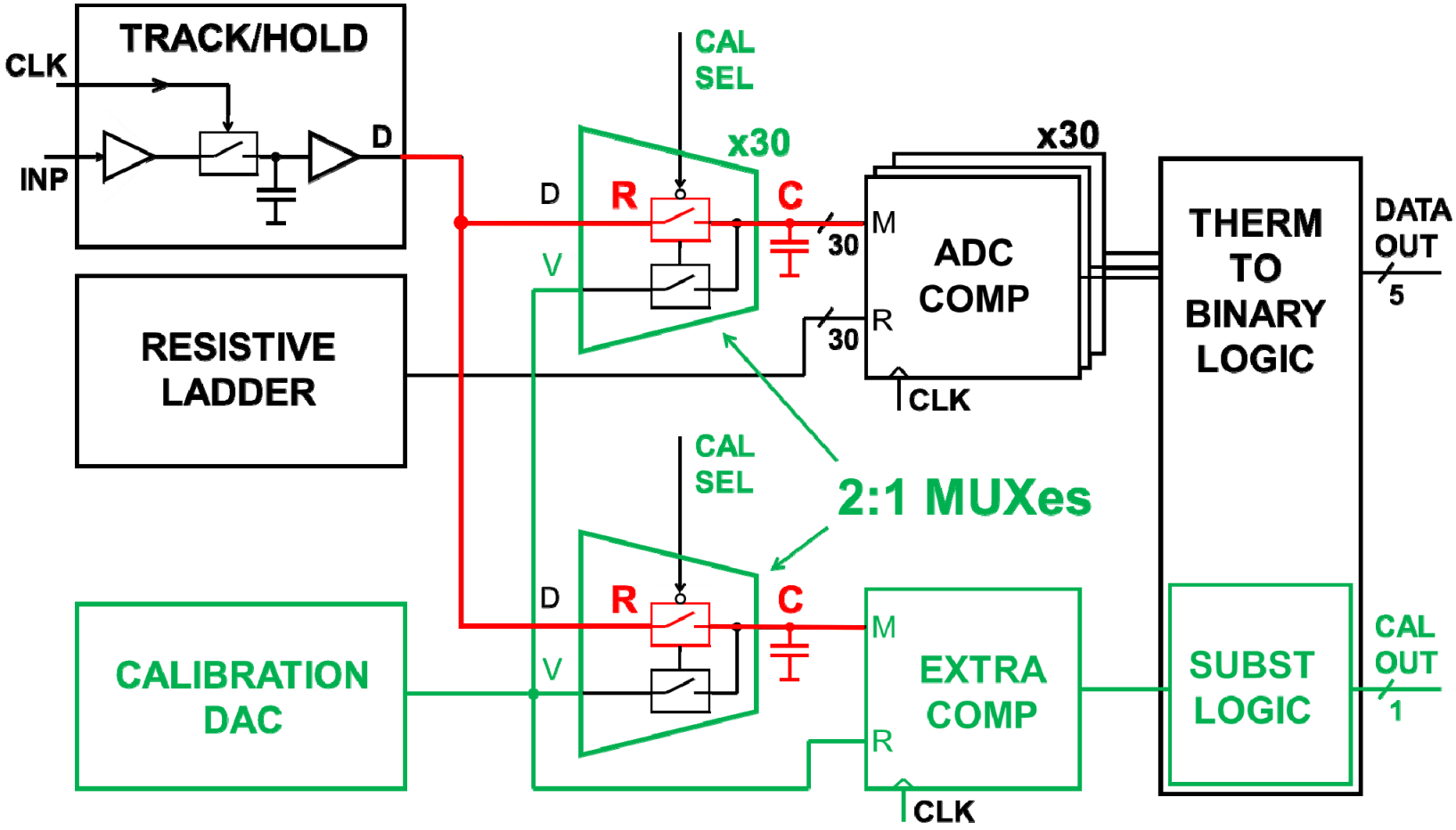
3. Add an extra "substitution" comparator with a 2:1 MUX

Self Calibration: Adding Substitution Logic



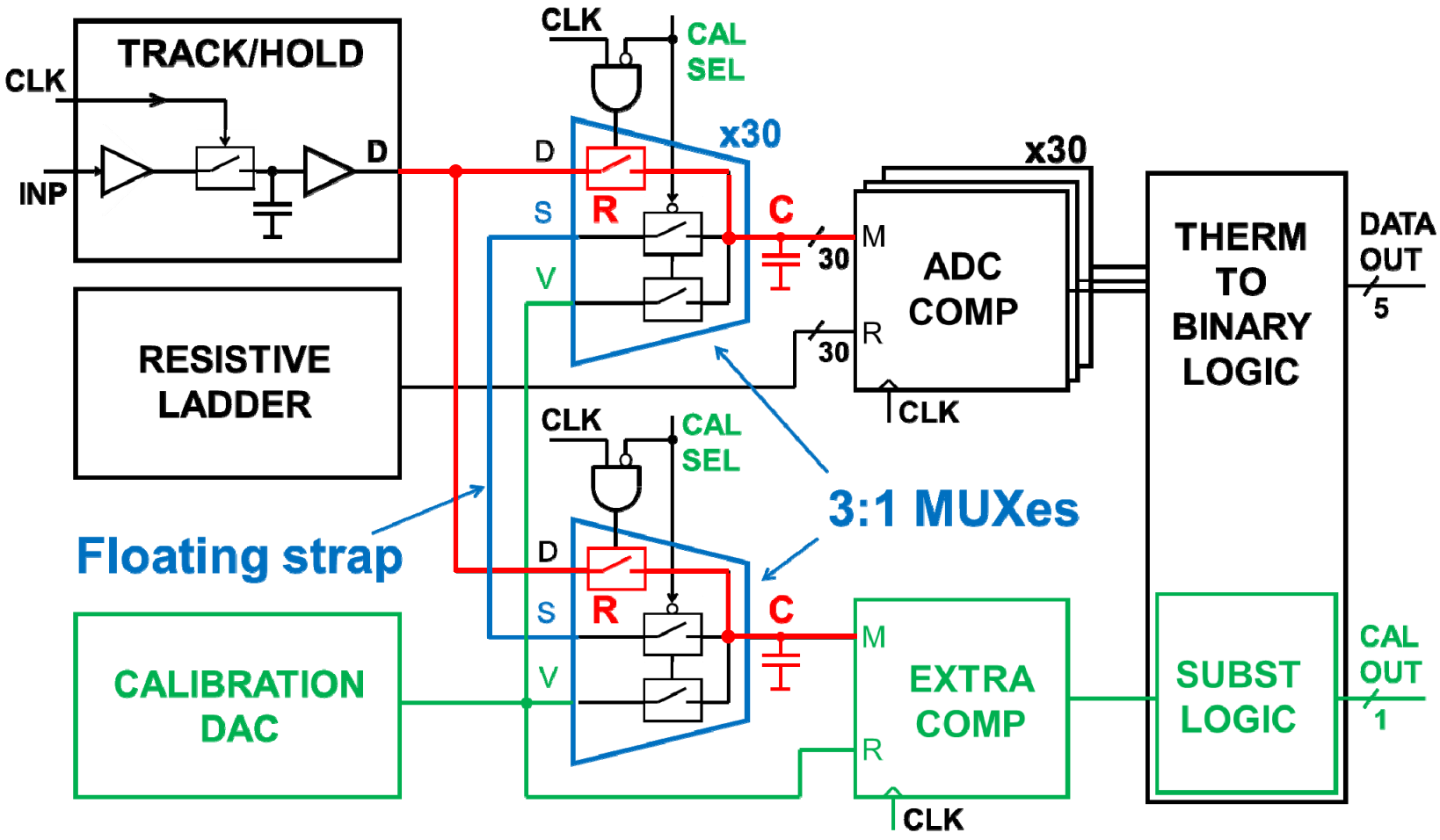
4. Add substitution logic to Thermometer-to-Binary logic block (for replacing comparator under calibration)

Self Calibration: Problem of Switch RC



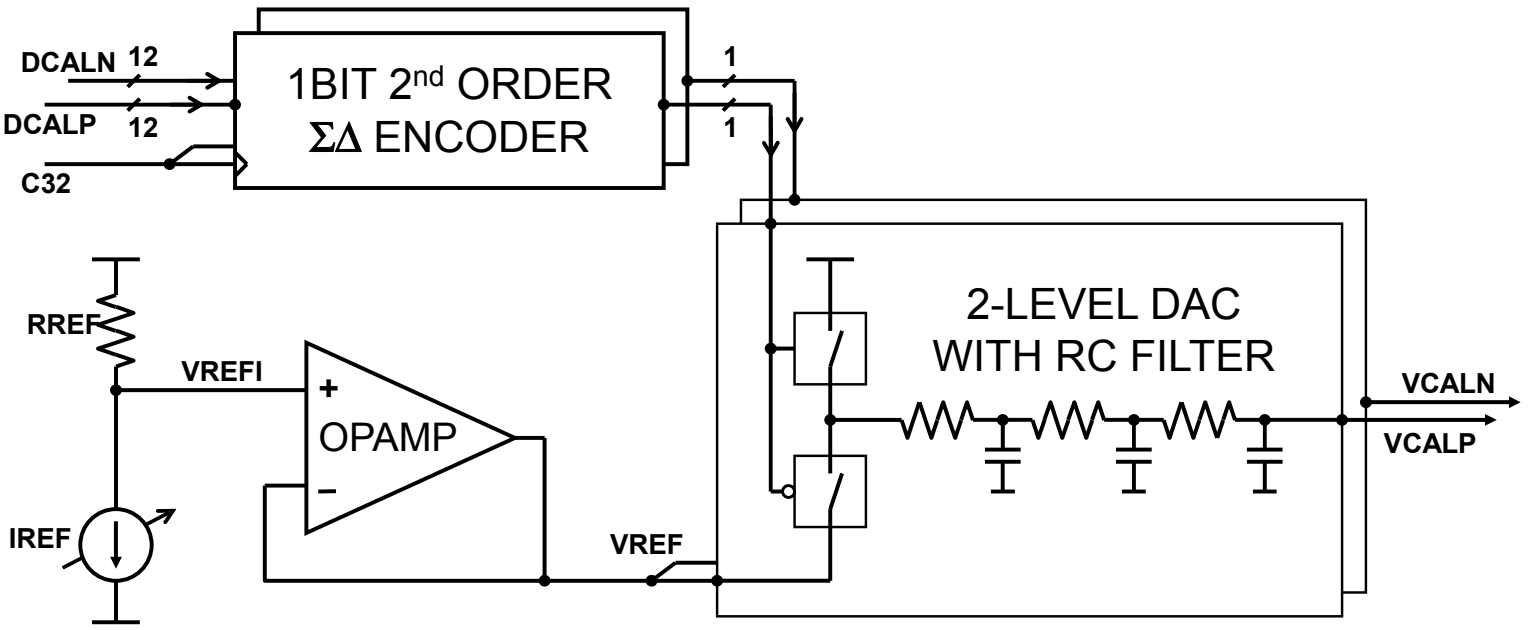
Problem: resistive switches in data path slow down settling, low-cost slave T/H stage is needed (to extend hold time x2)

Solution: Passive Slave T/H Stage



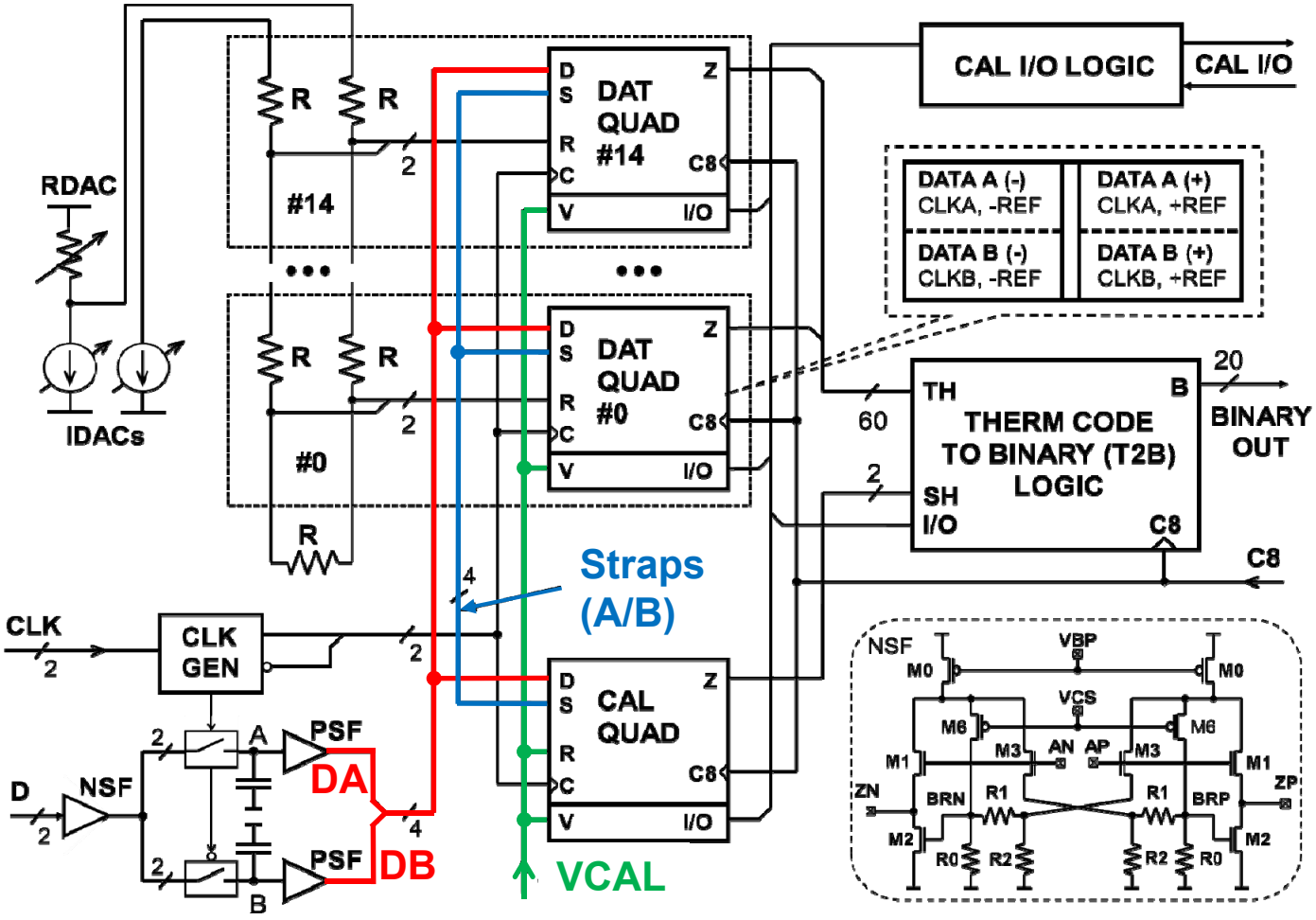
Solution: create passive slave stage by clocking existing switches and add floating strap for charge hold robustness

Architecture of CALDAC



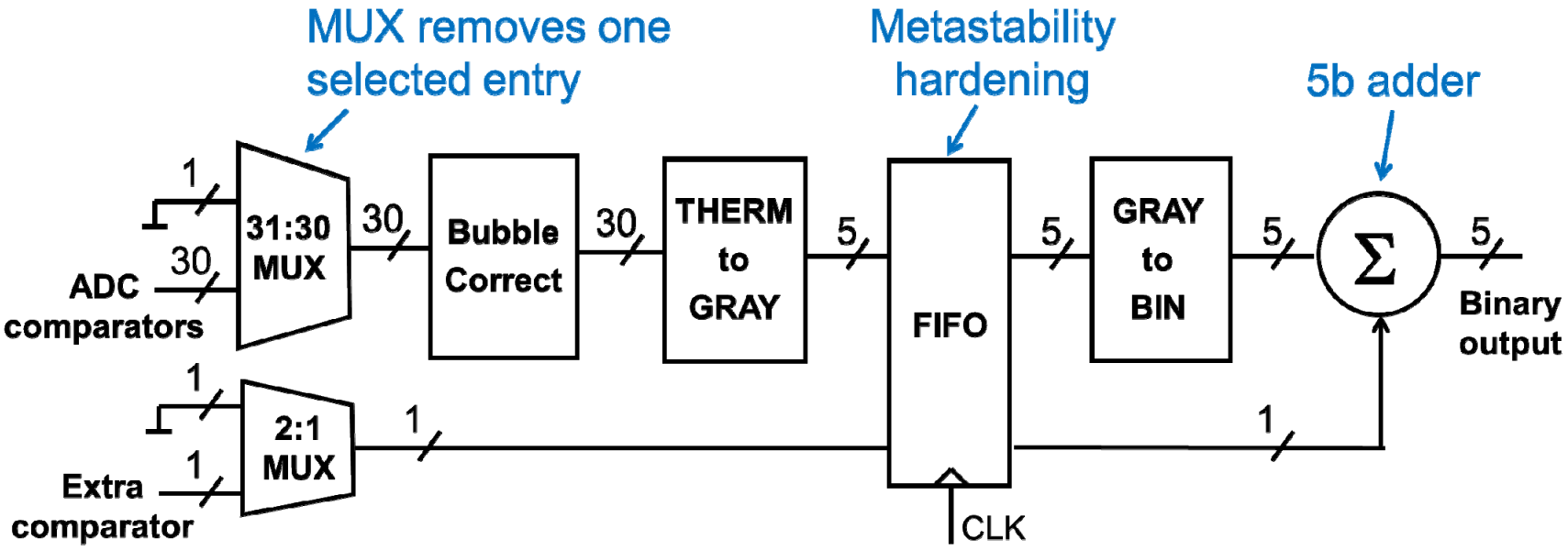
- **Sets precise target position of ADC thresholds**
- **Uses a pair of single-ended 12b DACs, each made of 1b 2nd order sigma-delta encoder, 1b DAC and 3-stage passive RC filter**

Architecture of Half-ADC



- Each half-ADC uses two complementary clock phases (A,B)
- Contains two sets of 30 comparators (and 2 extra ones)

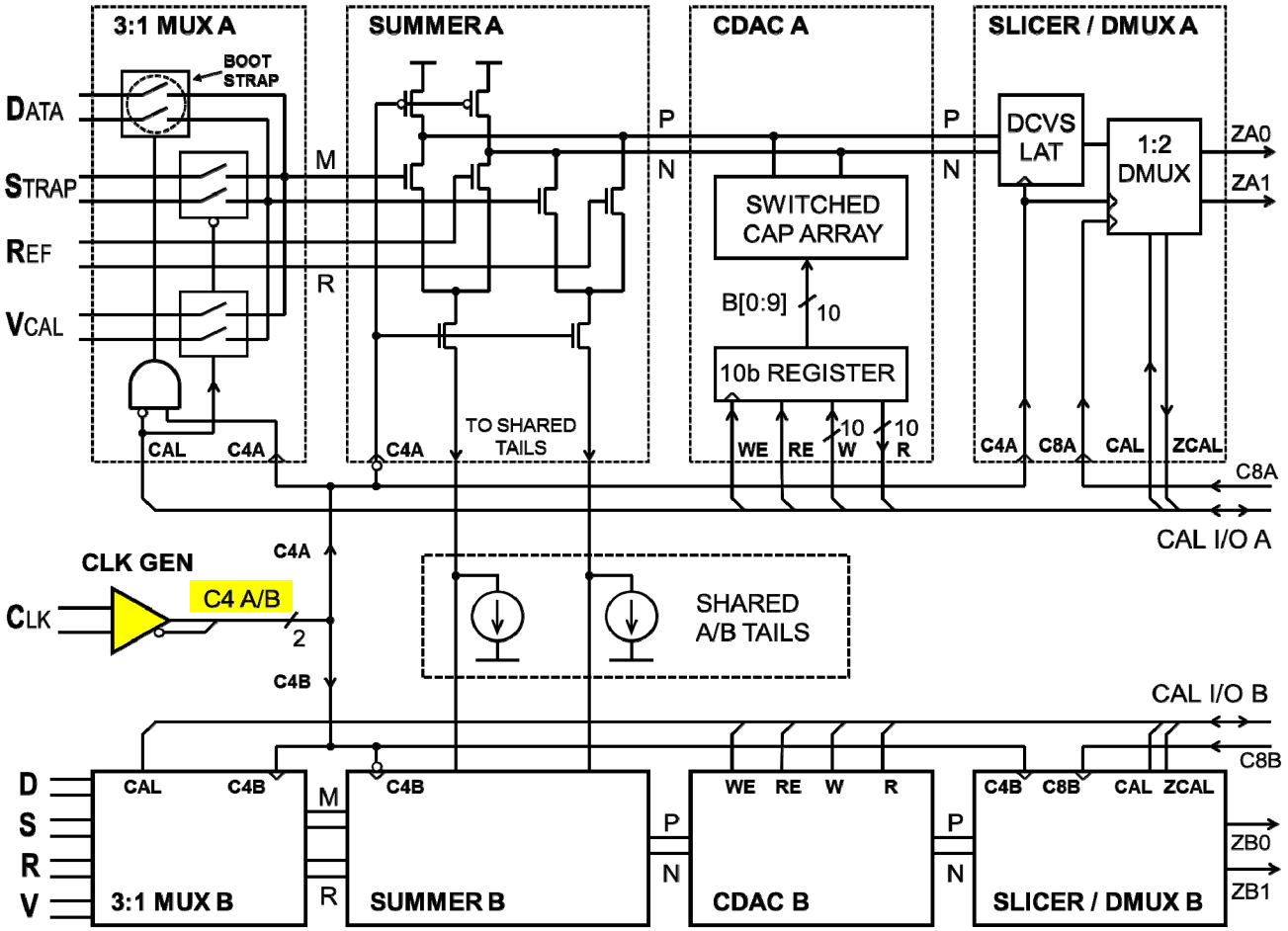
Thermometer-to-Binary Block



Performs two independent functions:

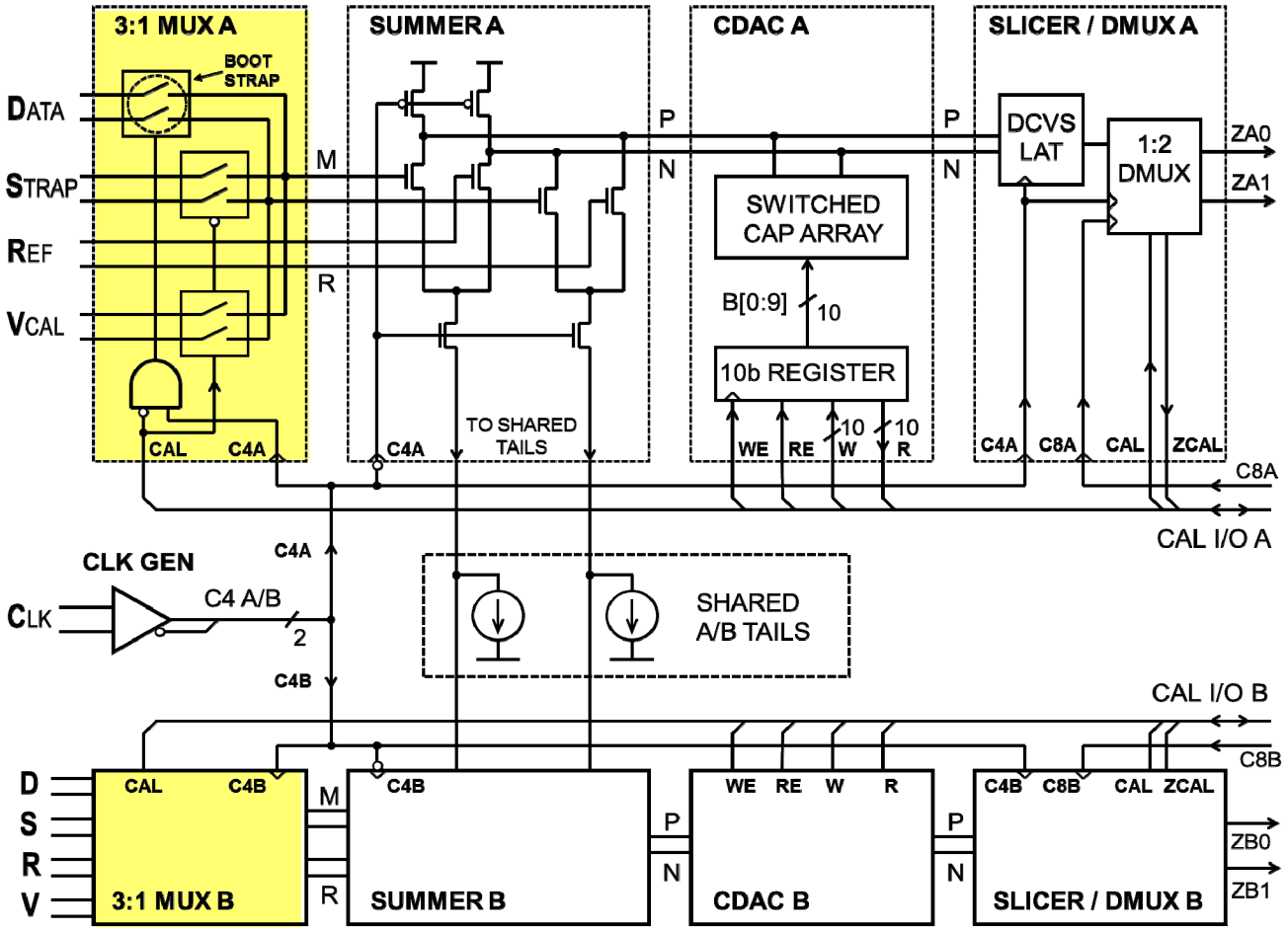
- computes metastability-hardened 5b binary output from outputs of 30 ADC comparators
- substitutes output of comparator under calibration with output of an extra comparator

Block Diagram of a Comparator Pair



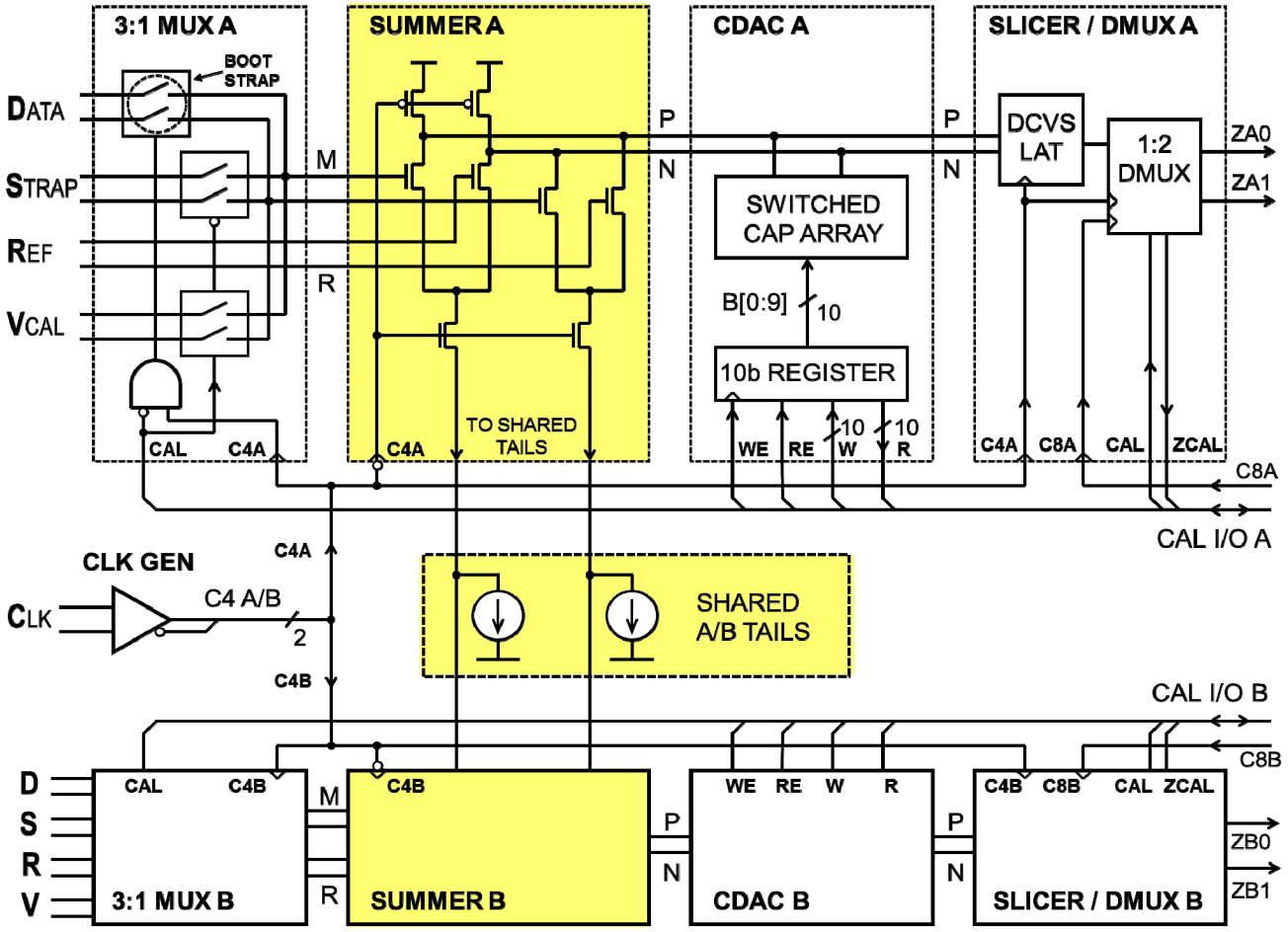
Two comparators in a pair are clocked with complementary clock phases (A/B) from a shared clock buffer

Comparator Block Diagram: 3:1 MUX



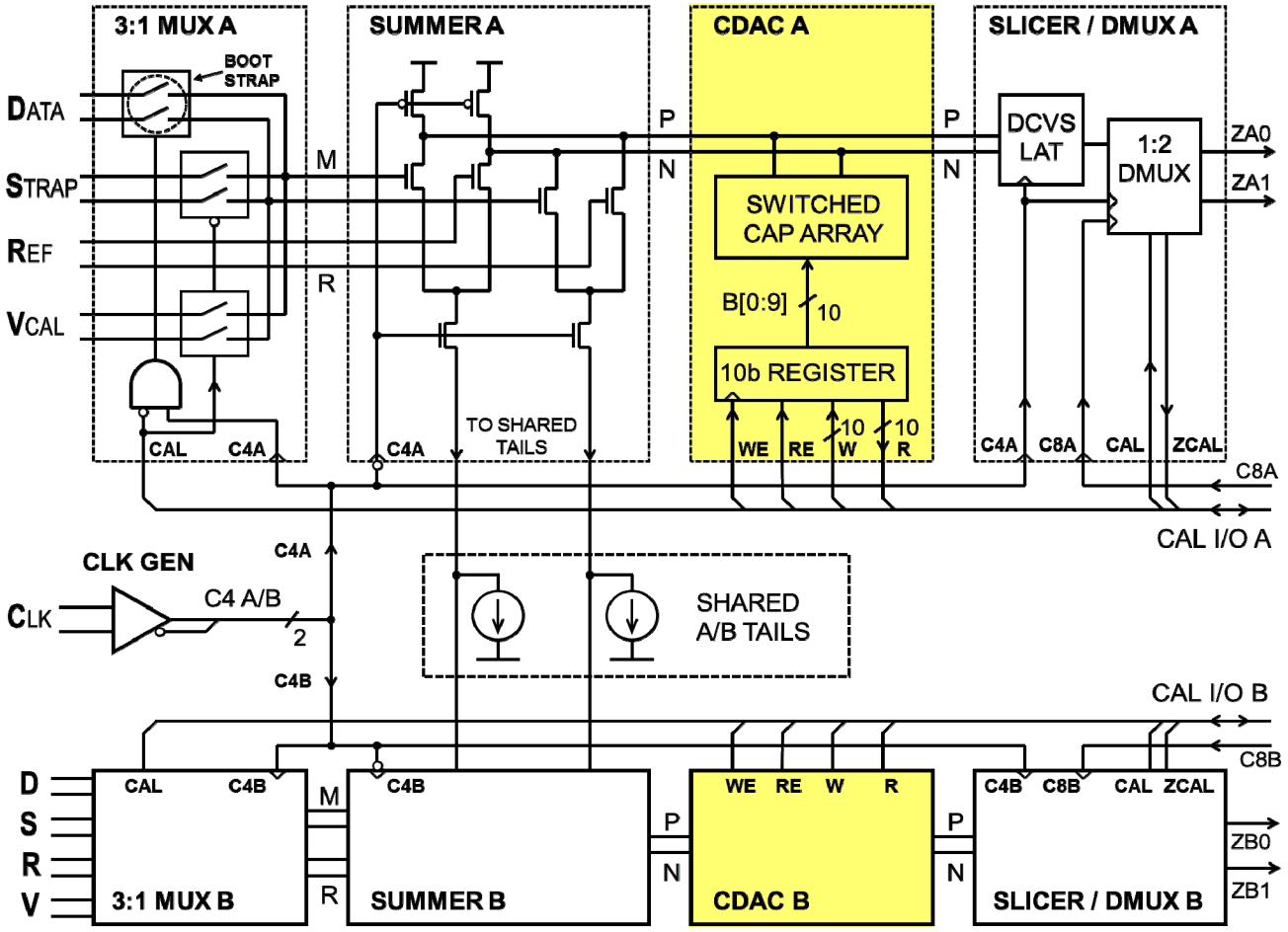
Each comparator is preceded by a clocked 3:1 MUX that enables ADC self-calibration and passive hold mode

Comparator Block Diagram: Summer



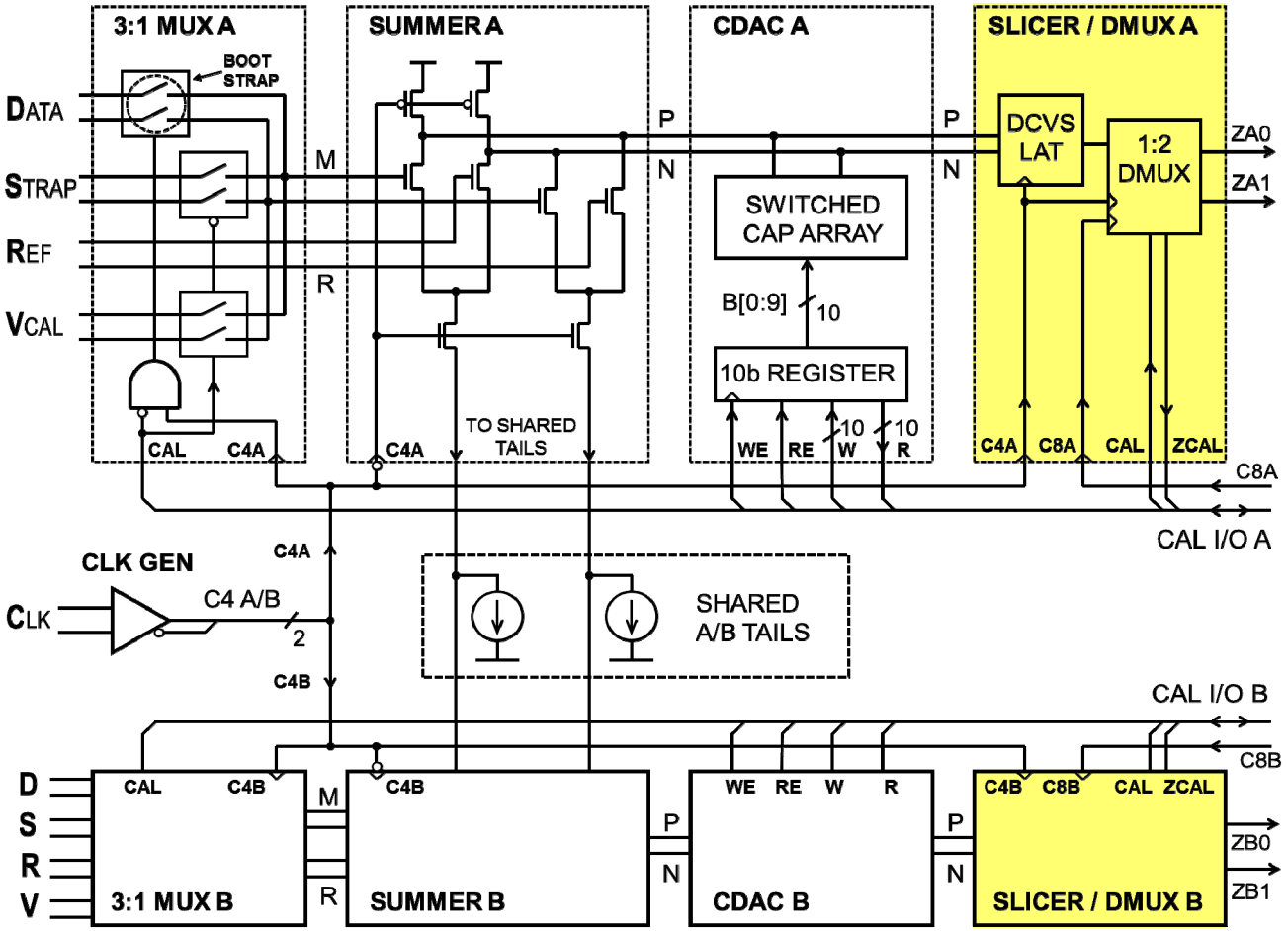
Integrating summers in the comparator pair use shared current tails to save power

Comparator Block Diagram: CDAC



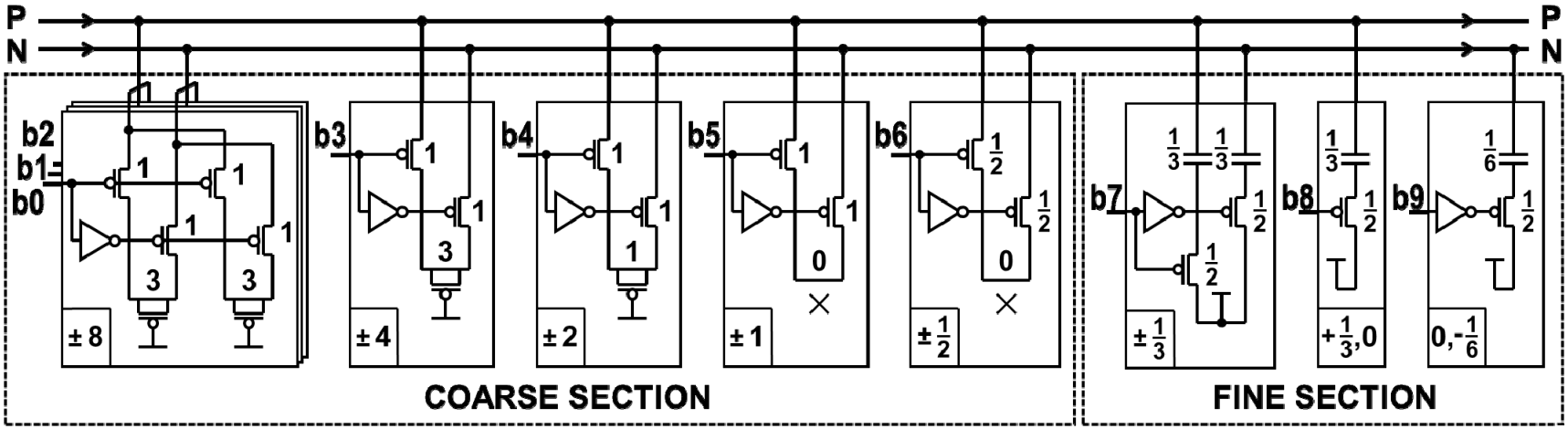
Passive 9b CDAC connects to summer output to control its offset over +/-80mV range with sub-mV precision

Comparator Block Diagram: Slicer



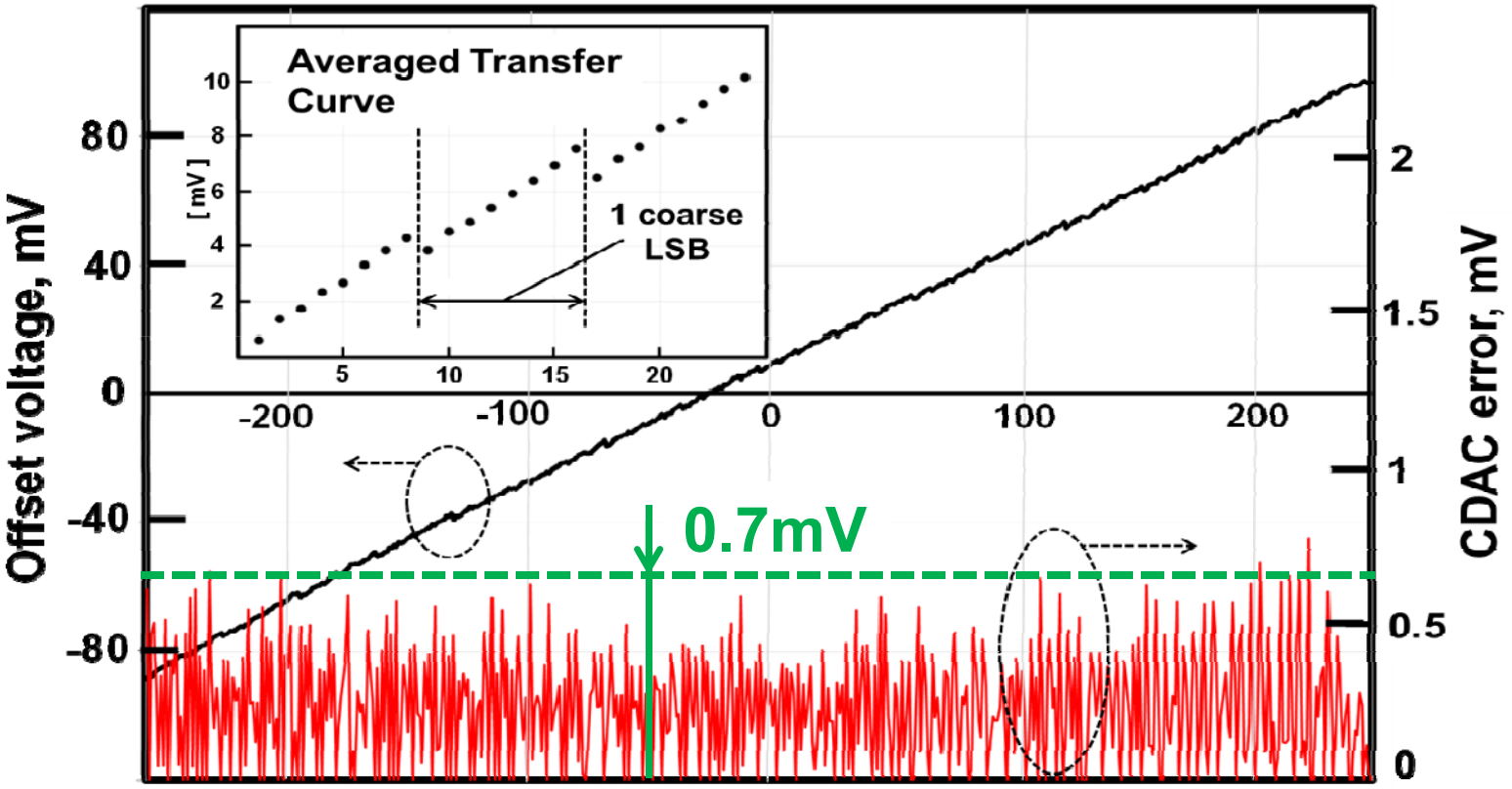
Slicer output is demultiplexed to 1/8 rate before applying it to Thermometer-to-Binary logic block

Schematic of 9-bit CDAC



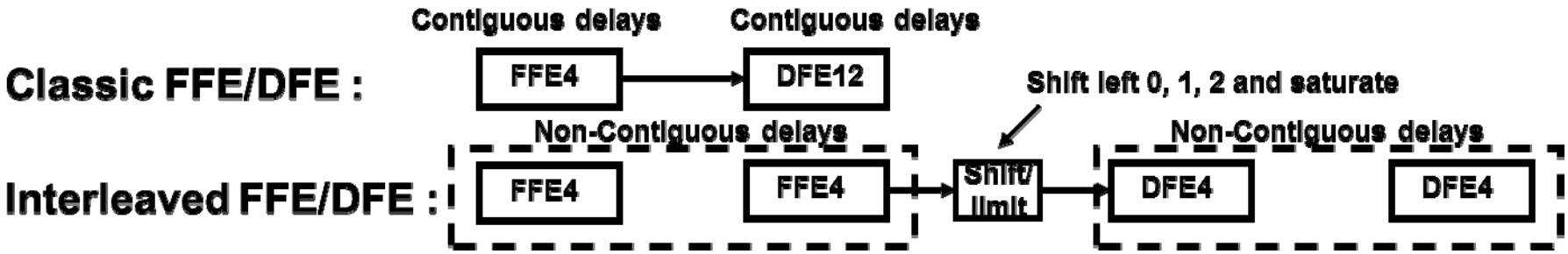
- Coarse section is composed of identical 1-finger PFETs used both as capacitors and as switches
- Fine section uses small wire caps in series with PFET switches
- Coarse LSB to fine MSB ratio (3:2) targets 0.5 bit coarse/fine range overlap for 8.5bit effective resolution

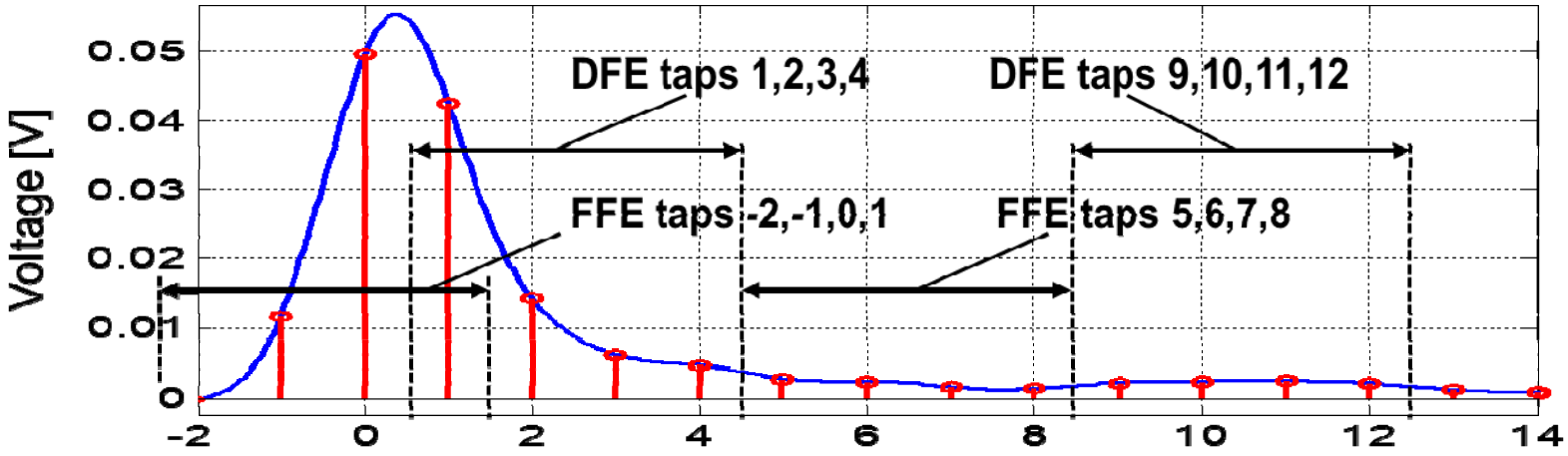
Measured Resolution of 9-bit CDAC



CDAC achieves sub-mV resolution over +/- 85 mV offset range (referred to summer input)

FFE/DFE Partition in DSP

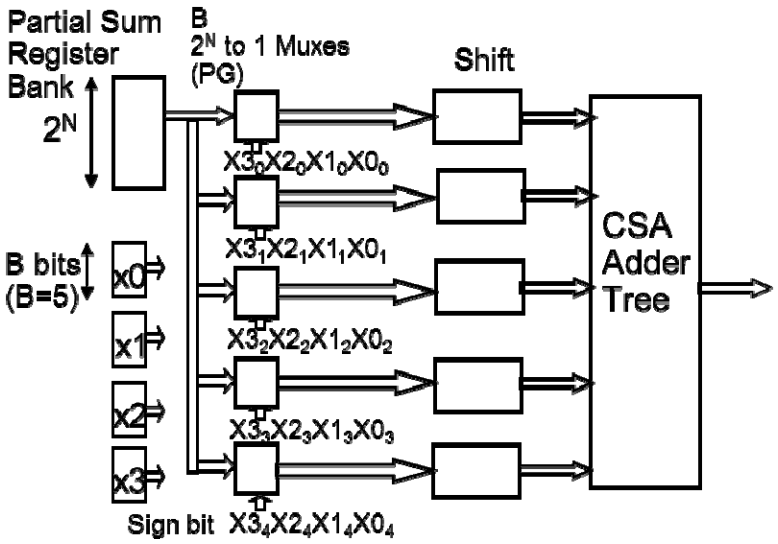




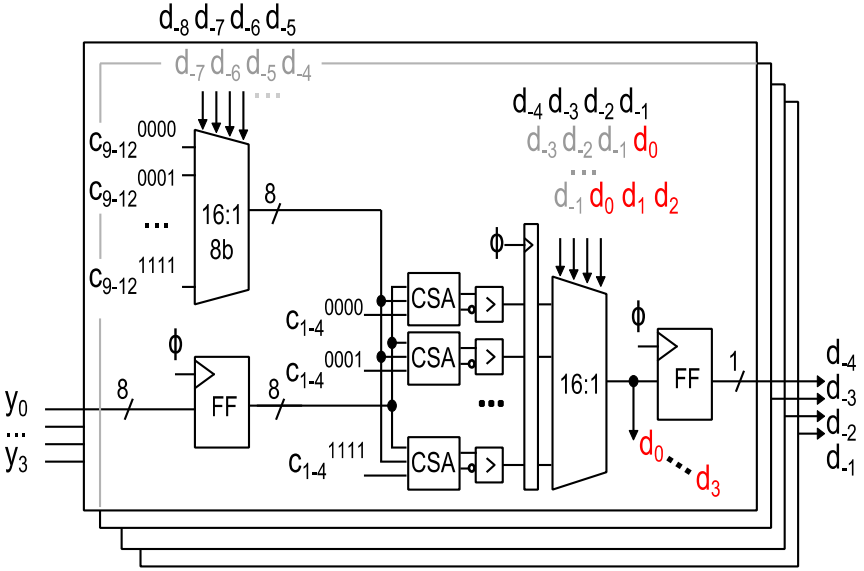
- Interleaved FFE8/DFE8
- Covers 2 precursors and 12 postcursors

FFE/DFE Architecture

Distributed-Arithmetic FFE



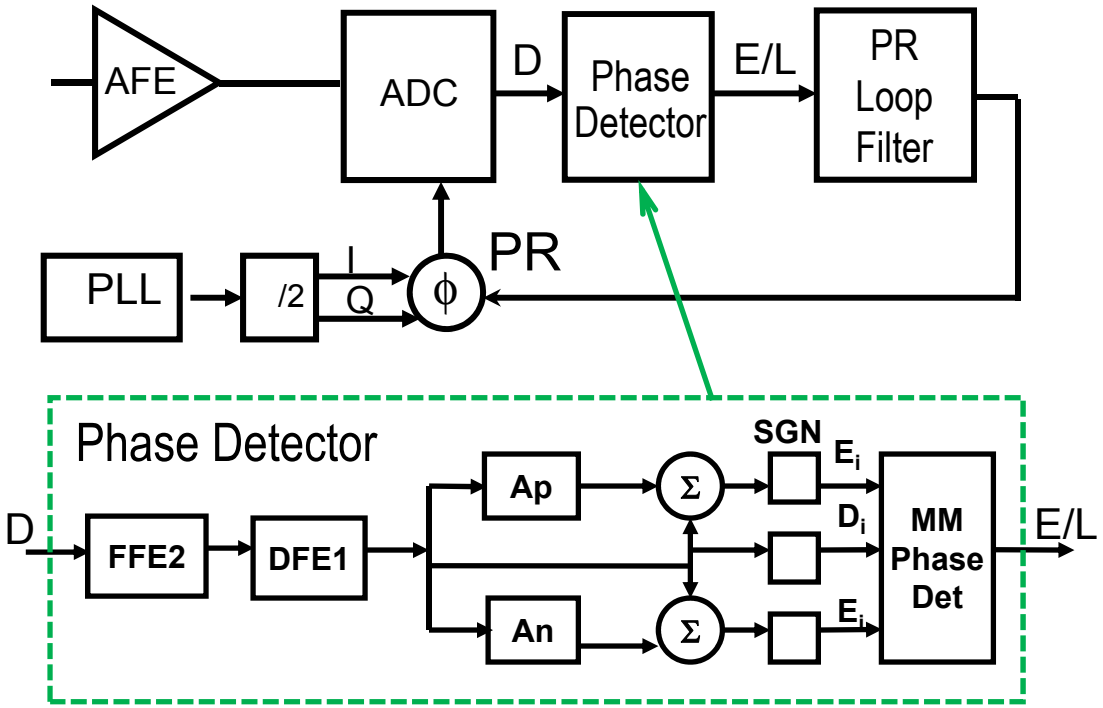
DFE



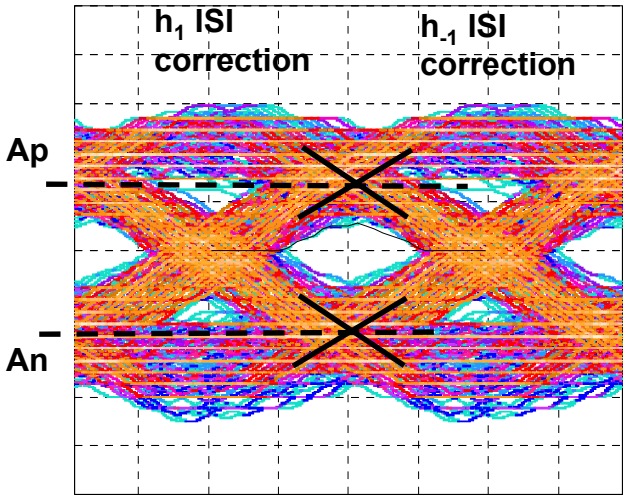
- **Full-Custom Distributed-Arithmetic FFE with 2^N=16 element partial sum lookup tables to eliminate need for multiplies[1]**
- **DFE uses full speculation for taps 1:4, direct feedback for taps 9:12 to minimize power, area and complexity[1]**

[1]T. Toifl et al., "A 3.5 pJ/bit 8-tap-feed-forward 8-tap-decision feedback digital equalizer for 16Gb/s I/Os", *ESSCIRC 2014, pp. 455-458*, Sept. 2014.

CDR Architecture

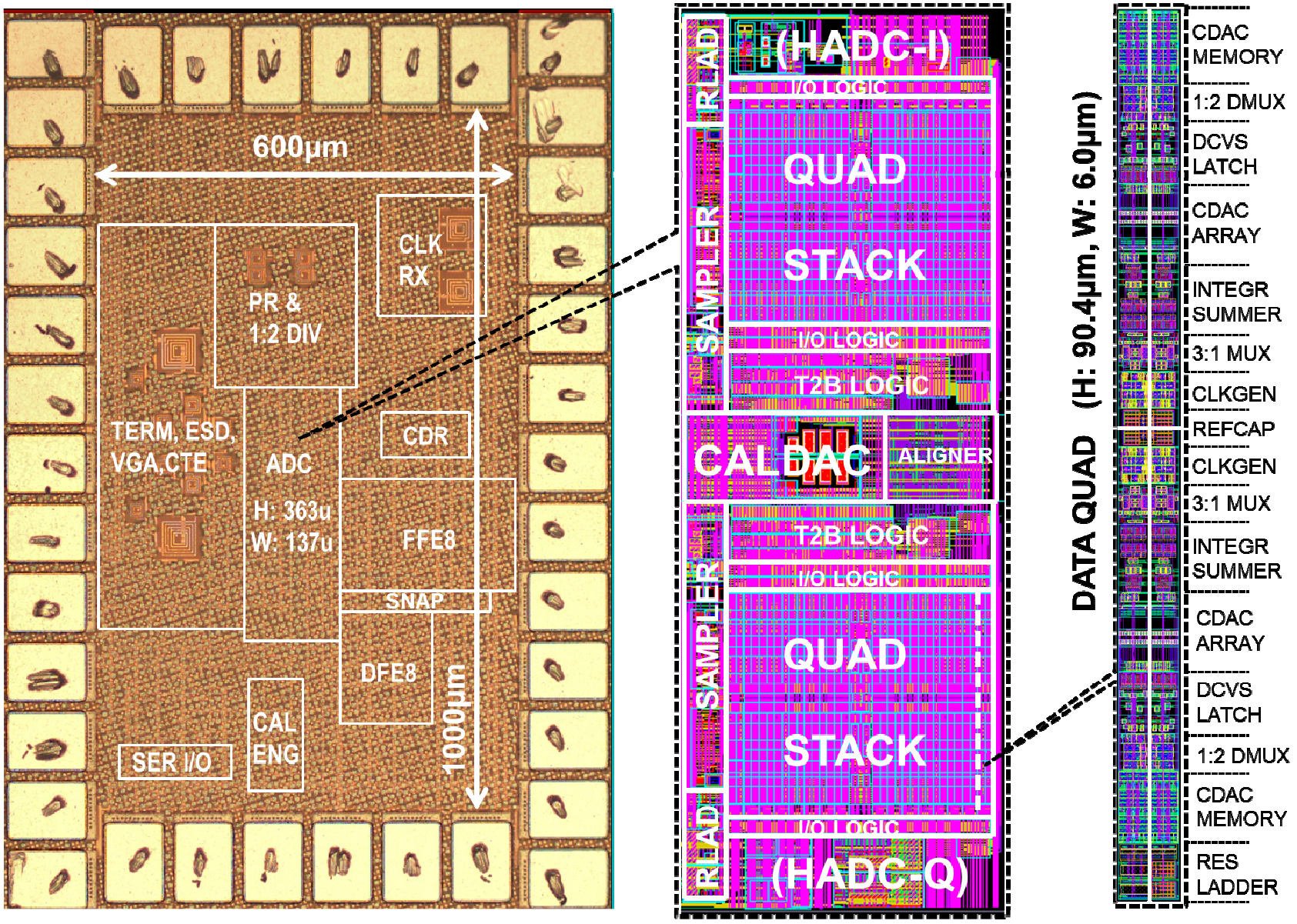


$$E\{D_{i-1}E_i - D_iE_{i-1}\} = 0$$



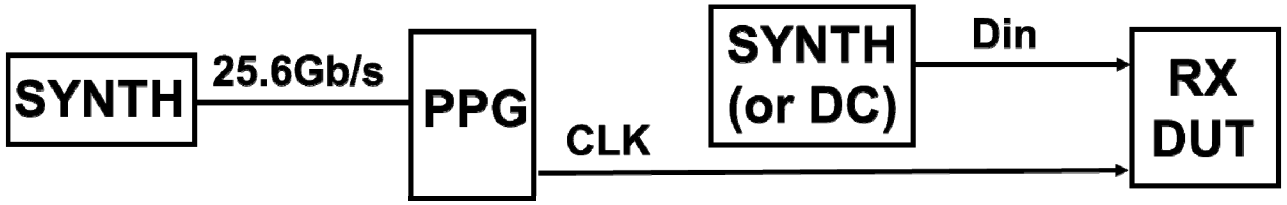
- **Local short FFE + DFE to reduce CDR loop latency followed by Muller-Mueller phase detector and PR control loop**
- **MM Phase detector locks to a timing point where postcursor ISI and precursor ISI are balanced, optimally at 0 ISI**

Chip Photo and ADC Layout

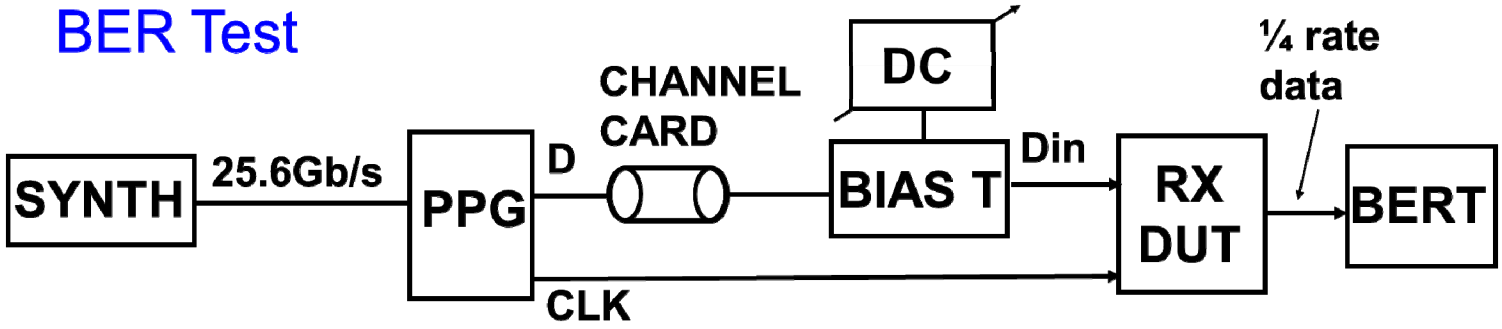


Receiver Test Setups

ENOB/DC Tests



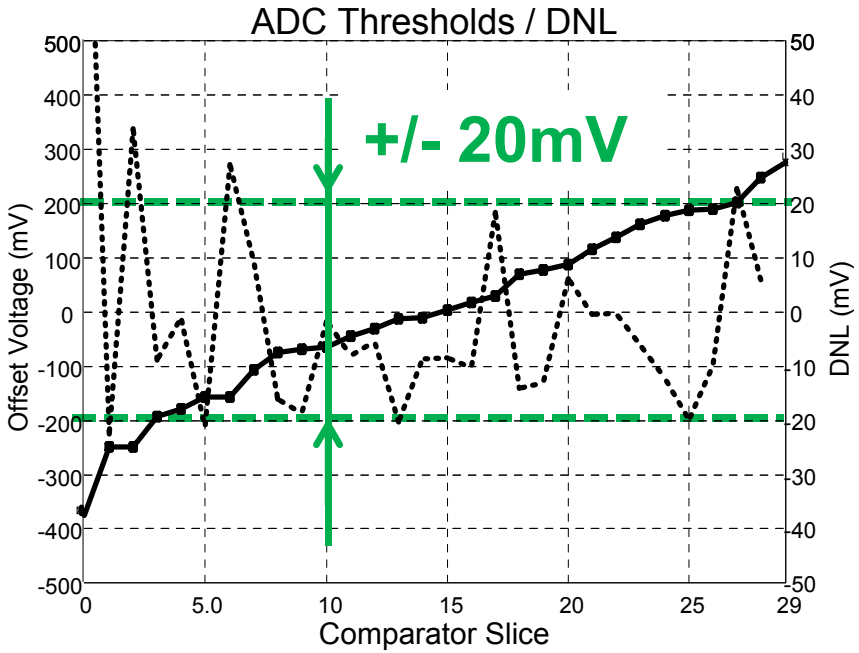
BER Test



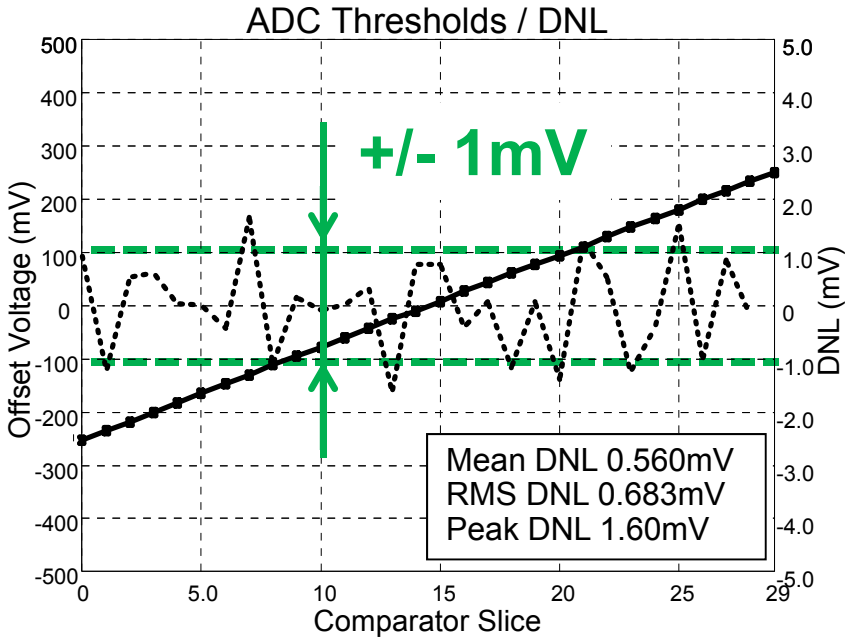
- Separate ADC ENOB and Rx BER setups
- Bias T added to channel in BER setup to enable high-resolution in-situ channel measurement with the Receiver
- Probe station used to connect to Rx pad cage

ADC DNL (Off-chip Calibration)

Uncalibrated DNL



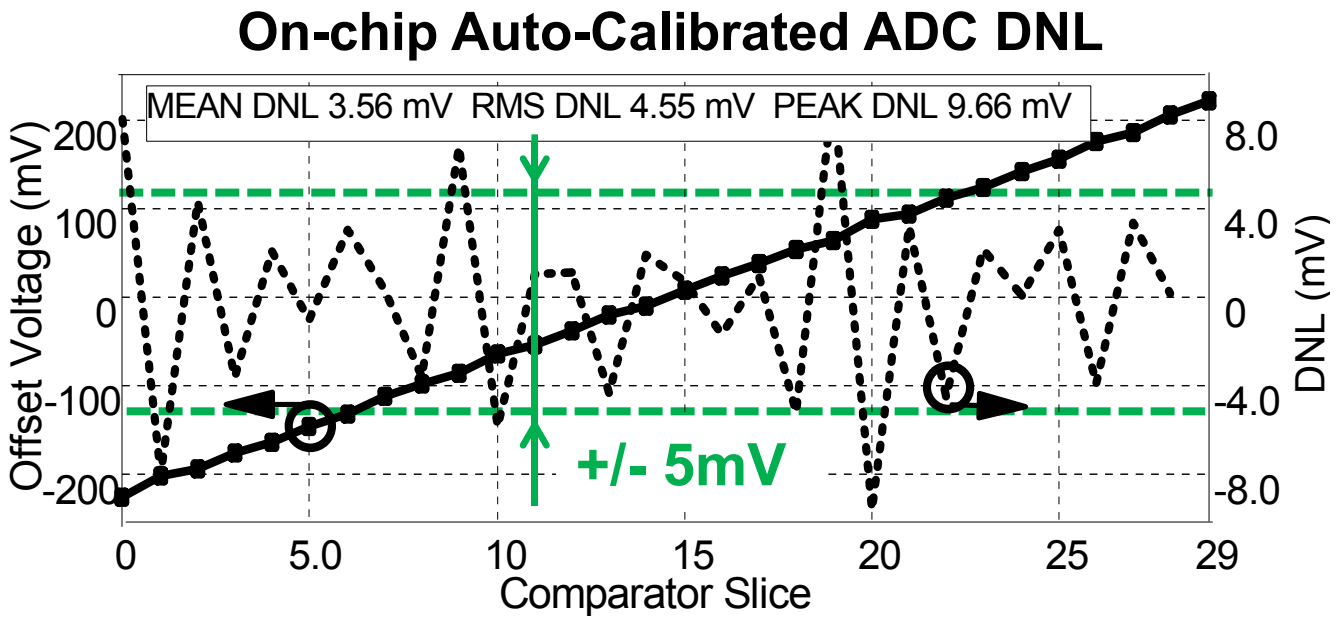
Off-chip calibrated DNL



ADC LSB: ~15mV

- **Uncalibrated DNL exceeds +/- 20mV**
- **Use of high-precision CDAC enables ~1mV calibrated DNL**

ADC DNL (On-chip Calibration)

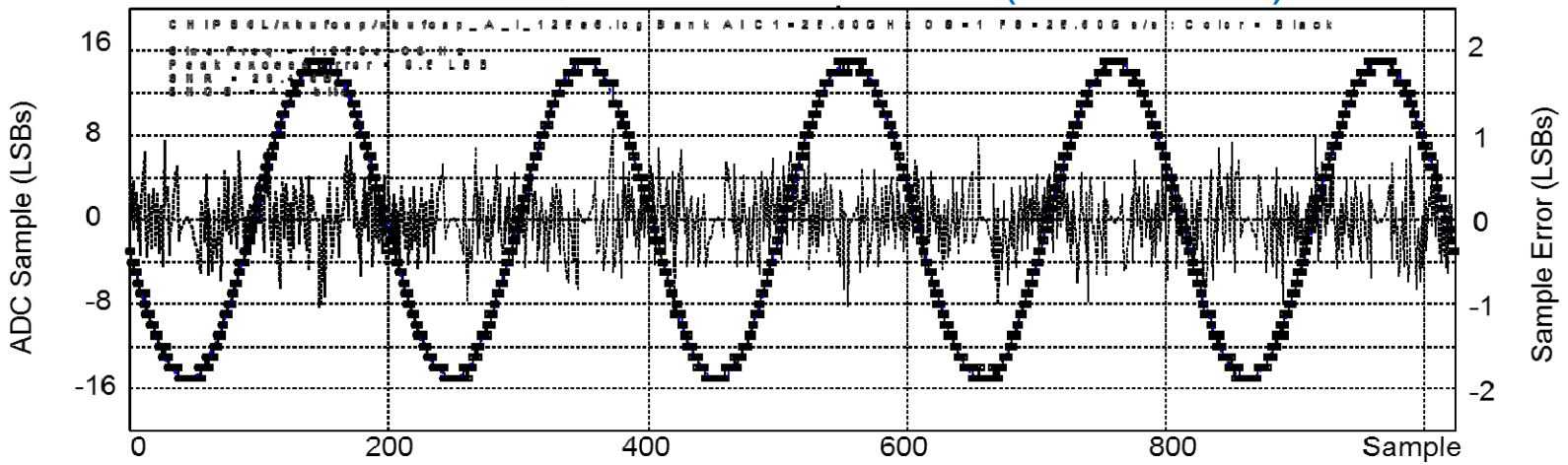


On-chip calibration results in x5 larger DNL vs off-chip calibration. It arises from:

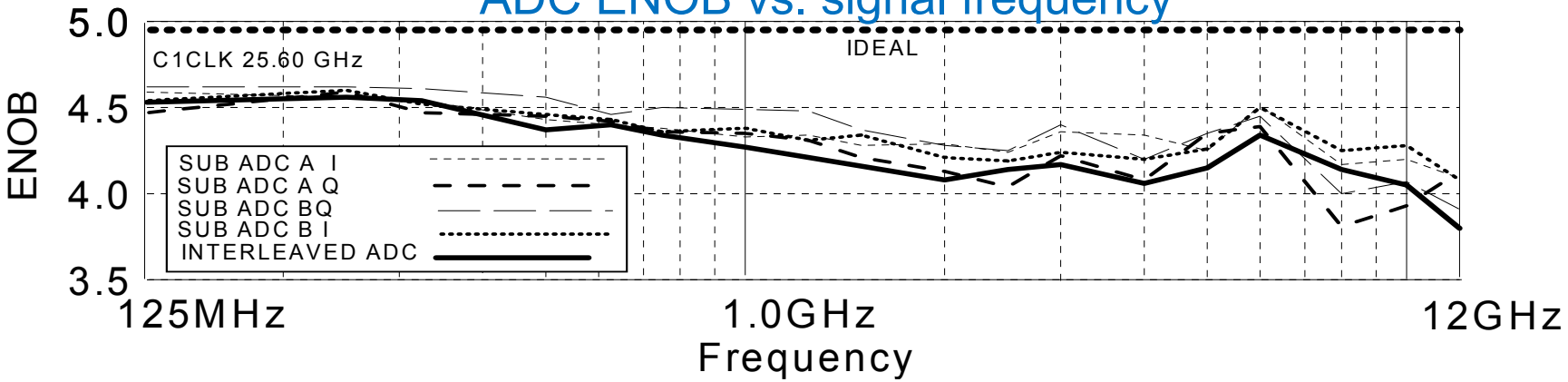
- **Insufficient averaging in the CAL logic state machine**
- **CAL port not being held stable to ~1mV accuracy by high output impedance CALDAC**

ADC ENOB at 25.6 GS/s

Conversion of 125 MHz sinewave (ENOB=4.5)

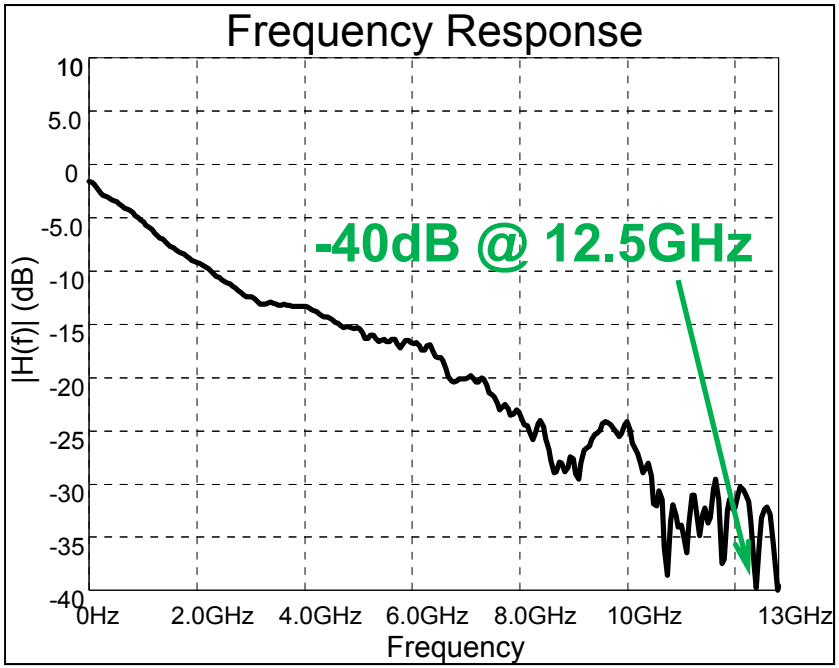


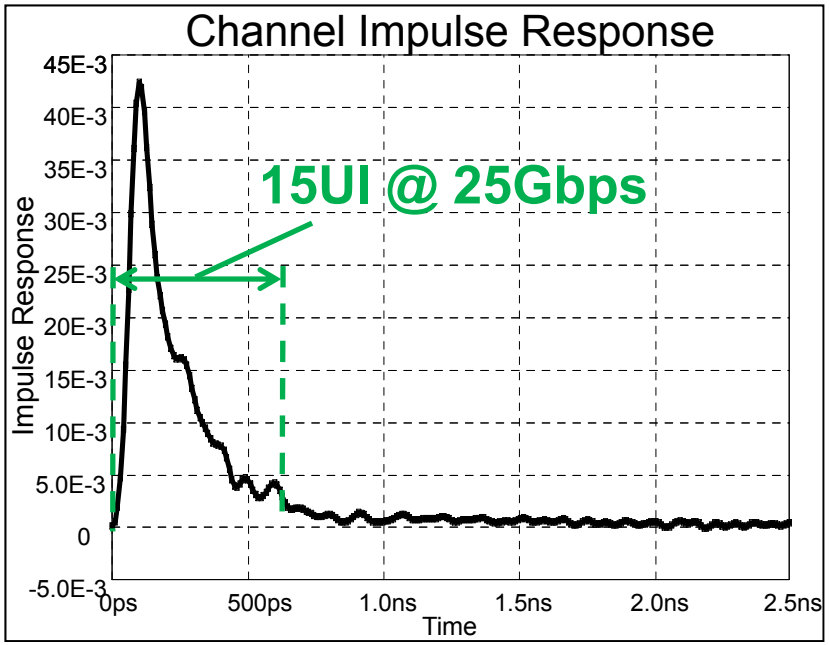
ADC ENOB vs. signal frequency



- **Low-frequency ENOB loss attributed to thermal noise**
- **Mid-band ENOB loss attributed to slew-rate limit in PSF**

30i 40dB loss Channel Response

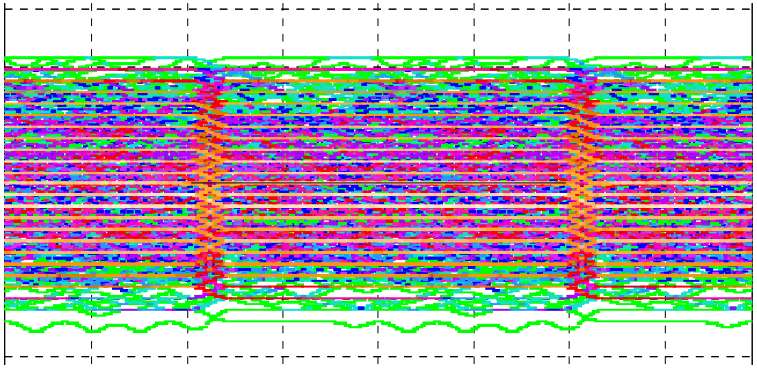




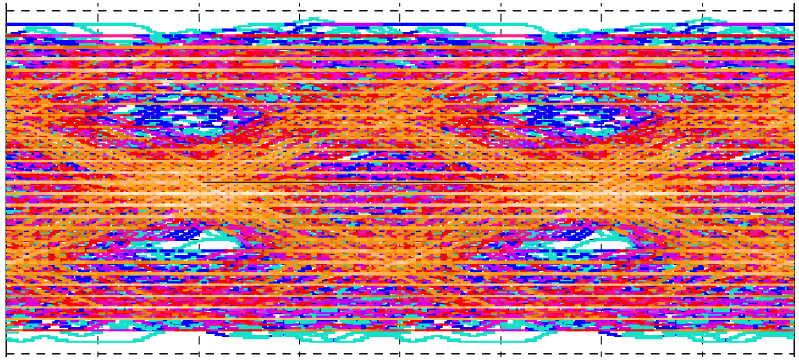
In-situ 40dB loss test channel: frequency response and time-domain impulse response

Equalization of a 40dB Loss Channel

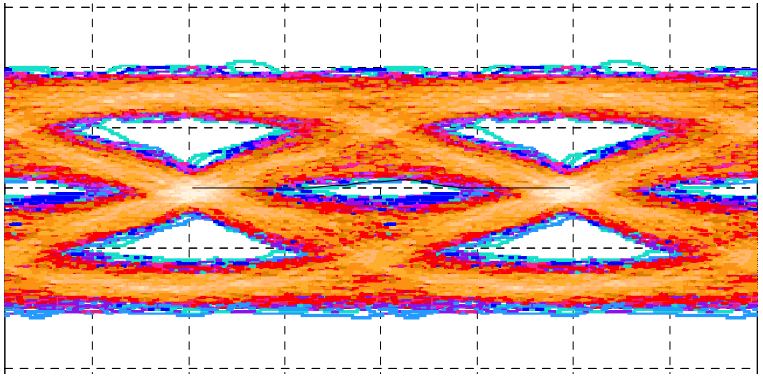
25.6Gb/s Eye No CTE, No FFE, No DFE



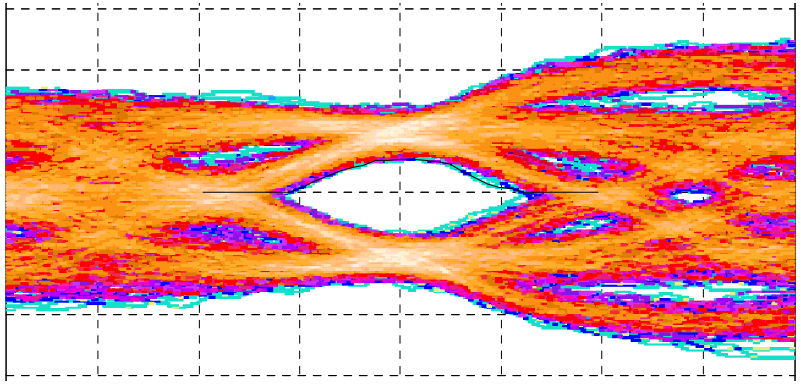
25.6Gb/s Eye CTE=max peak, No FFE, No DFE



25.6Gb/s Eye CTE=max peak, FFE8, No DFE

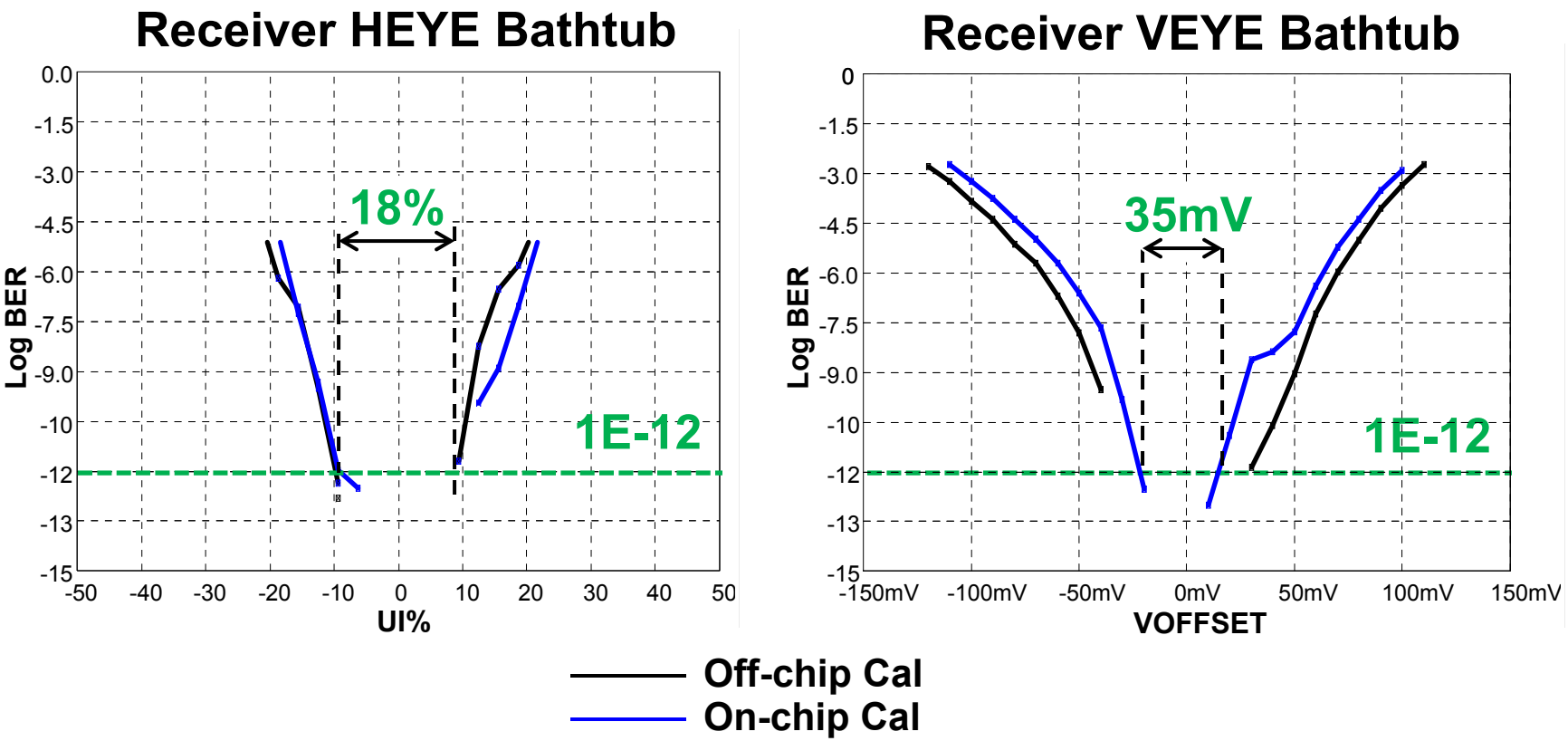


25.6Gb/s Eye CTE=max peak, FFE8, DFE8



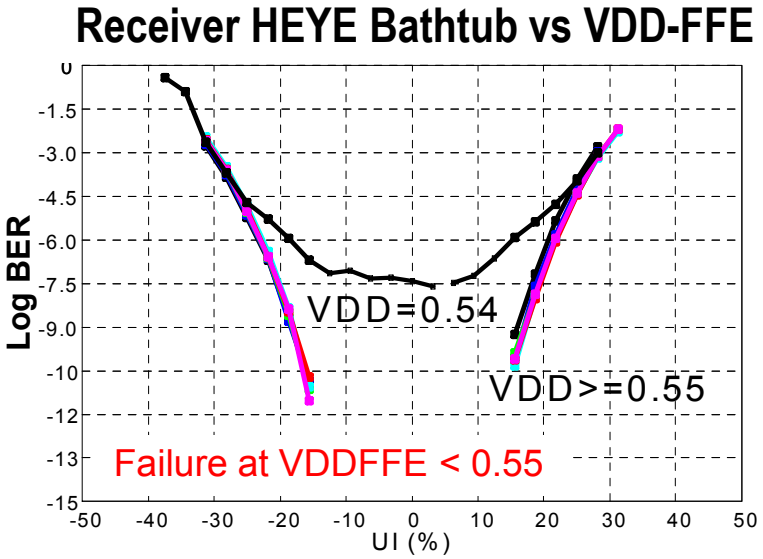
- CTE peaking reduces bulk channel loss
- Enabling digital FFE/DFE opens horizontal/vertical eye

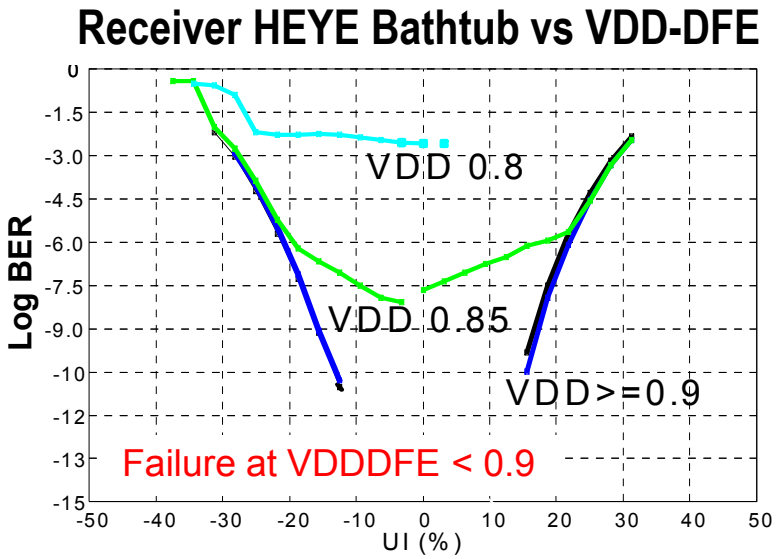
Receiver BER over 40dB Loss Channel

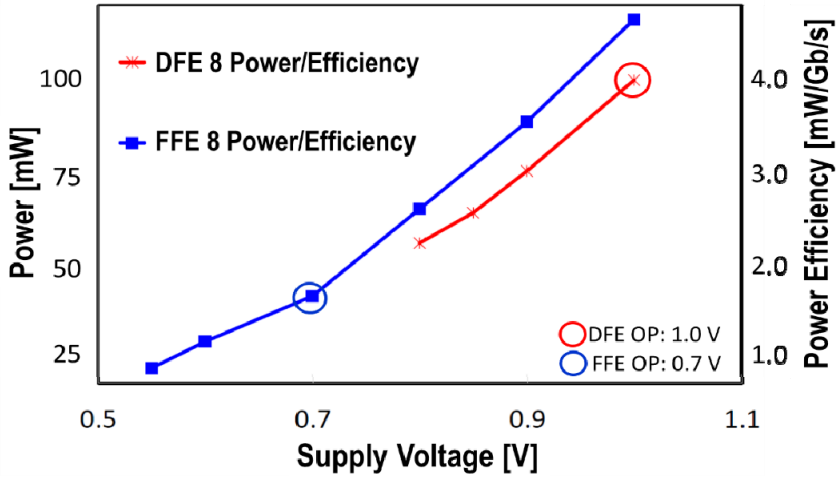


- Both on-chip and off-chip gain/offset calibration yield measurable Horizontal and Vertical eye margin at 1E-12 BER
- Extra 10mV DNL in on-chip calibration directly subtracts from vertical eye margin

25.6 Gb/s FFE8/DFE8 Operation vs VDD







FFE8 has x2 better power efficiency vs DFE8 due to lower VDD

Performance Summary

Technology	32nm CMOS SOI
Data Rate	25.6Gb/s
RX Equalization	8 tap FFE with 4+4 tap DFE
Area	0.39 mm^2
Supply Voltages	1.0V (for everything except FFE8 and ACC), 0.7V (for FFE8), 1.2V (for ACC)
RX input Sensitivity @ 25Gb/s	15mV_{pd} (for 1E-12 BER)
Horizontal eye opening @1E-12 BER, 40dB-Loss Channel	18% UI (7.8ps @ 25Gb/s)
Power @ 25 Gb/s	Analog+CDR: 310mW (from 1V) DFE: 100mW (from 1V) FFE: 43mW (from 0.7V) **Total: 453mW**

Conclusions

- We have demonstrated 25.6Gb/s digital serial link receiver with VGA/CTE, 5b flash ADC, FFE, DFE, and CDR designed in 32nm SOI CMOS
- Key focus areas of the design
  - ADC architecture that supports dynamic offset and gain calibration with high precision (~1mV) and low area overhead
  - Power efficient DSP techniques including distributed-arithmetic FFE and interleaved FFE/DFE
  - Low-latency baud-rate CDR
- The digital receiver achieved error-free (BER < 10^{-12}) operation at 25.6Gb/s in a lossy/reflective channel with 40 dB loss

Acknowledgments

- Members of IBM Research and Global Foundries High-Speed Serial (HSS) Group

- Specific IBM colleagues:

  M. Sanduleanu, JO Plouchart, J. Proesel, S. Dhawan, S. Kim, M. Kuppannan and A. Sahasrabuddhe

A 320mW 32Gb/s 8b ADC-Based PAM-4 Analog Front-End with Programmable Gain Control and Analog Peaking in 28nm CMOS

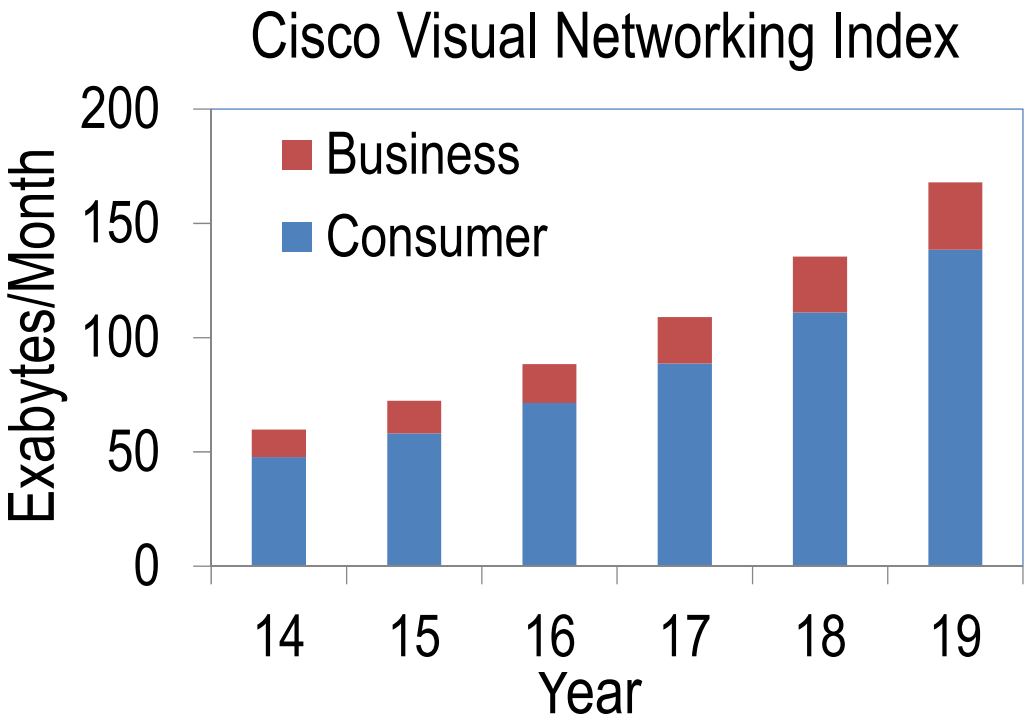
Delong Cui, Heng Zhang, Nick Huang, Ali Nazemi, Burak Catli, Hyo Gyuem Rhew, Bo Zhang, Afshin Momtaz, Jun Cao

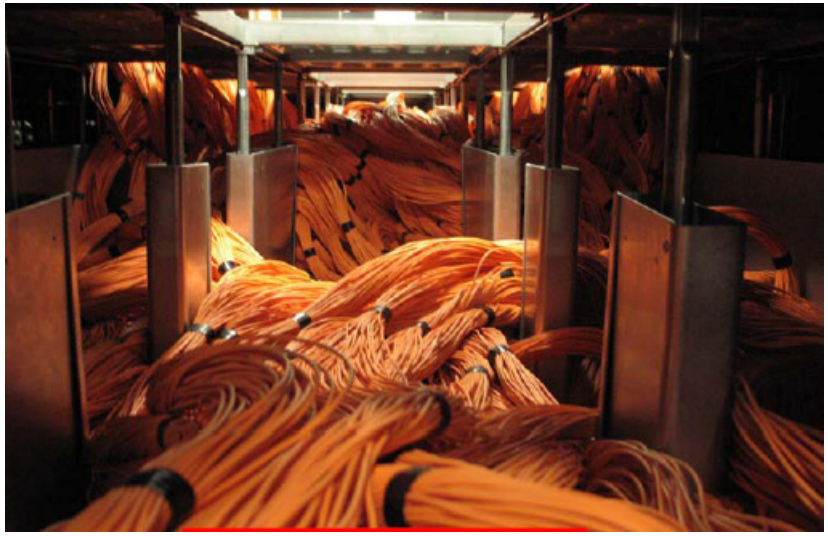
Broadcom, Irvine, CA

Outline

- Introduction
- ADC-based Analog Front-End Architecture
- Circuit Implementation
- Measurement Results
- Comparison and Summary

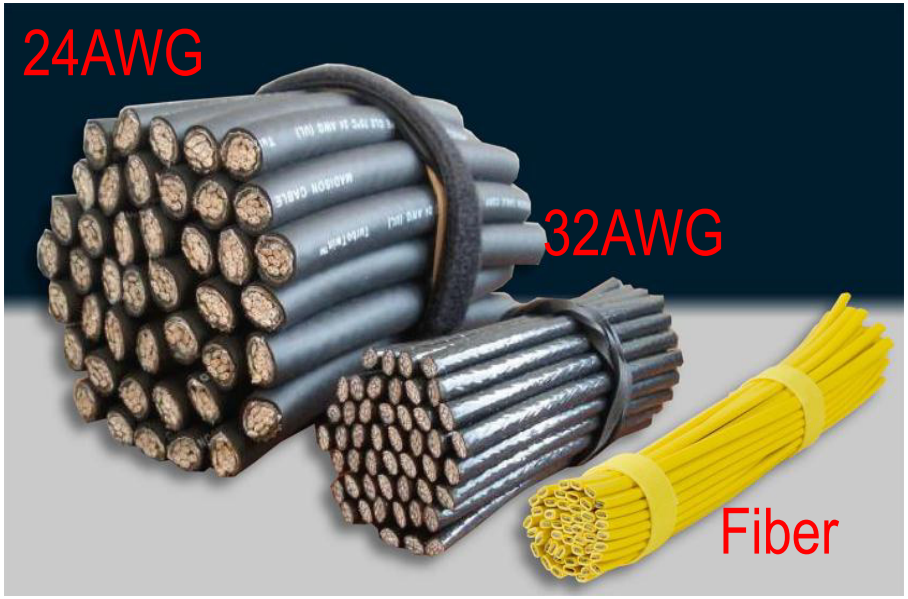
Global IP Traffic Growth

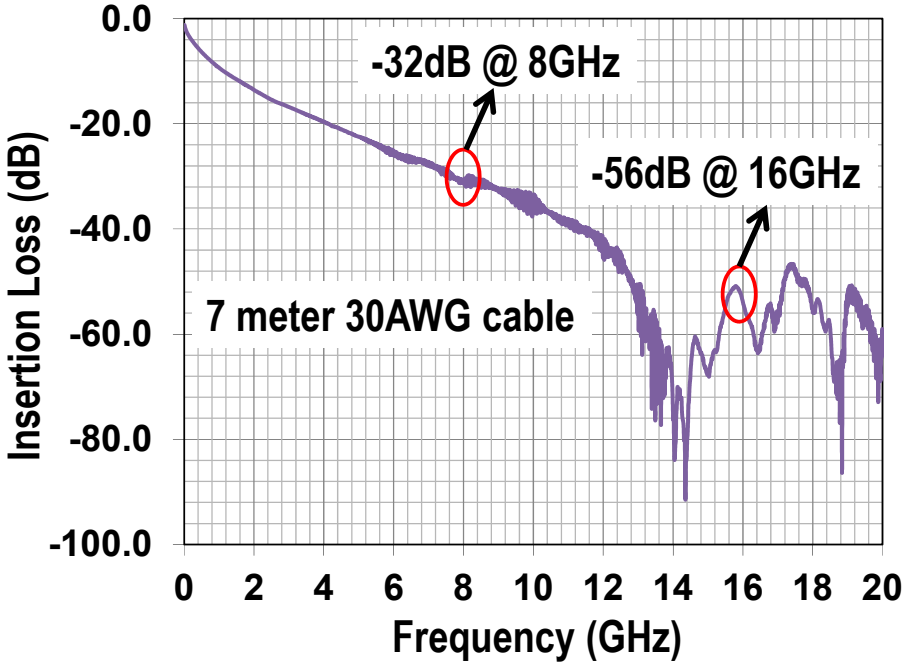




- Global internet traffic will nearly triple from 2014 to 2019
- Higher data rate transmission required to reduce the number of cables needed

Multi-Level Signaling Format



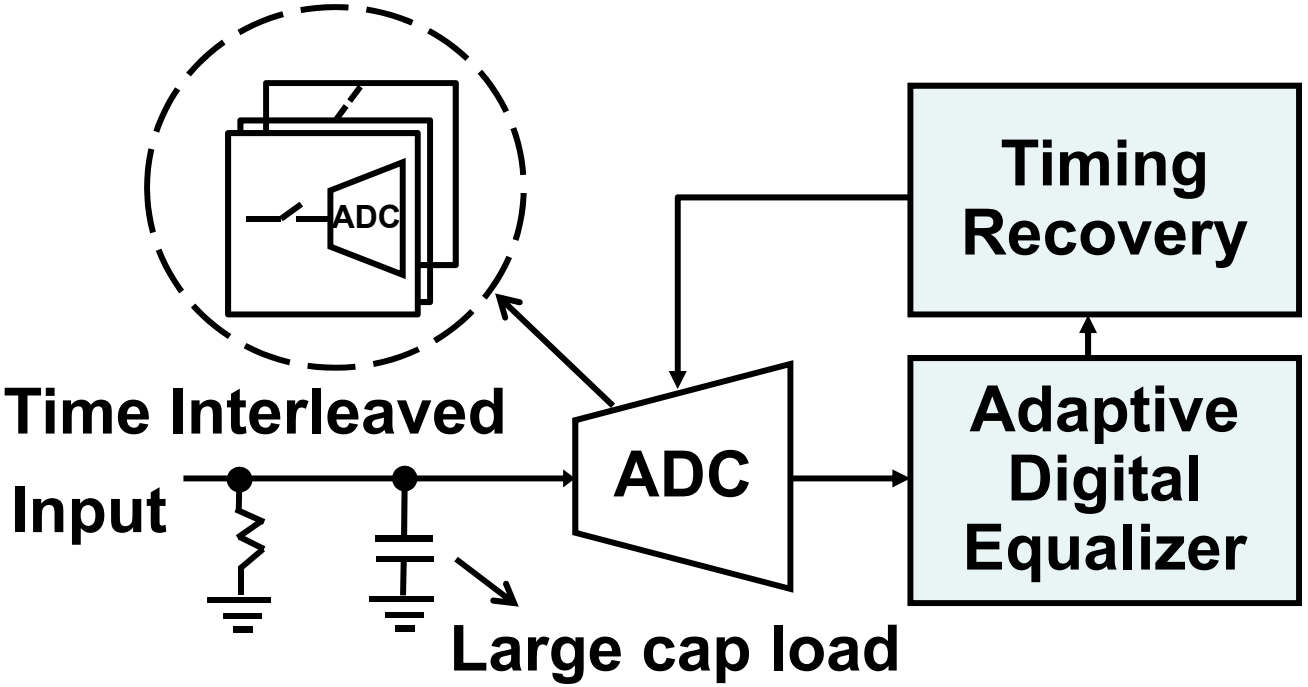


- Multi-Level signaling format, such as PAM4 is needed as the data rate increases
  - Significantly more loss for NRZ versus PAM4
  - PAM4 becomes more efficient with >30Gbps data rate

Challenges with PAM4 Format

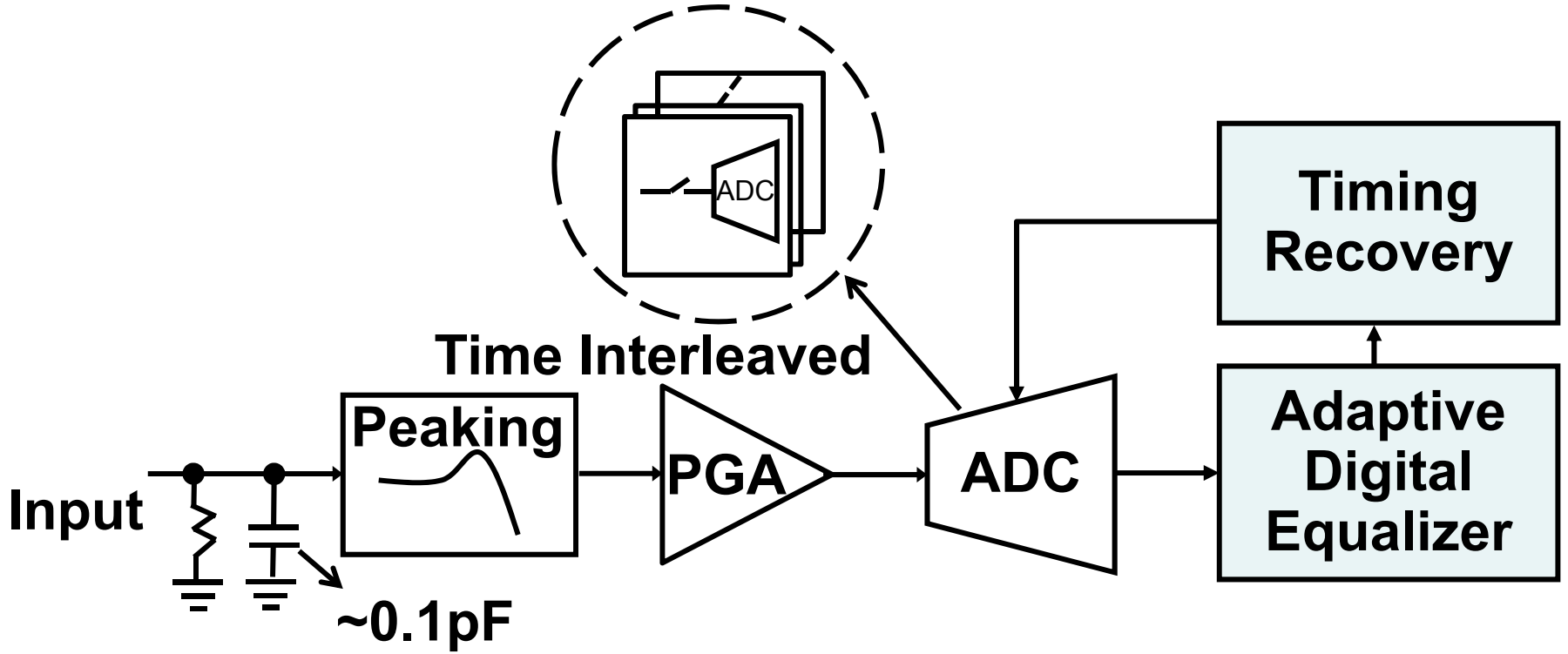
- Advantages
  - *Relaxation of cable loss requirement*
    - *Two bits per symbol/Reduction of Nyquist*
- Challenges
  - *Signal attenuated by 9.5dB*
  - *The signal loss must be compensated*
  - *More sensitive to noise, reflection and nonlinearity*
- ADC based solution
  - *Inherently compatible with multi-level signaling*
  - *ADC/DSP combination compensates more loss*

ADC Based Solution



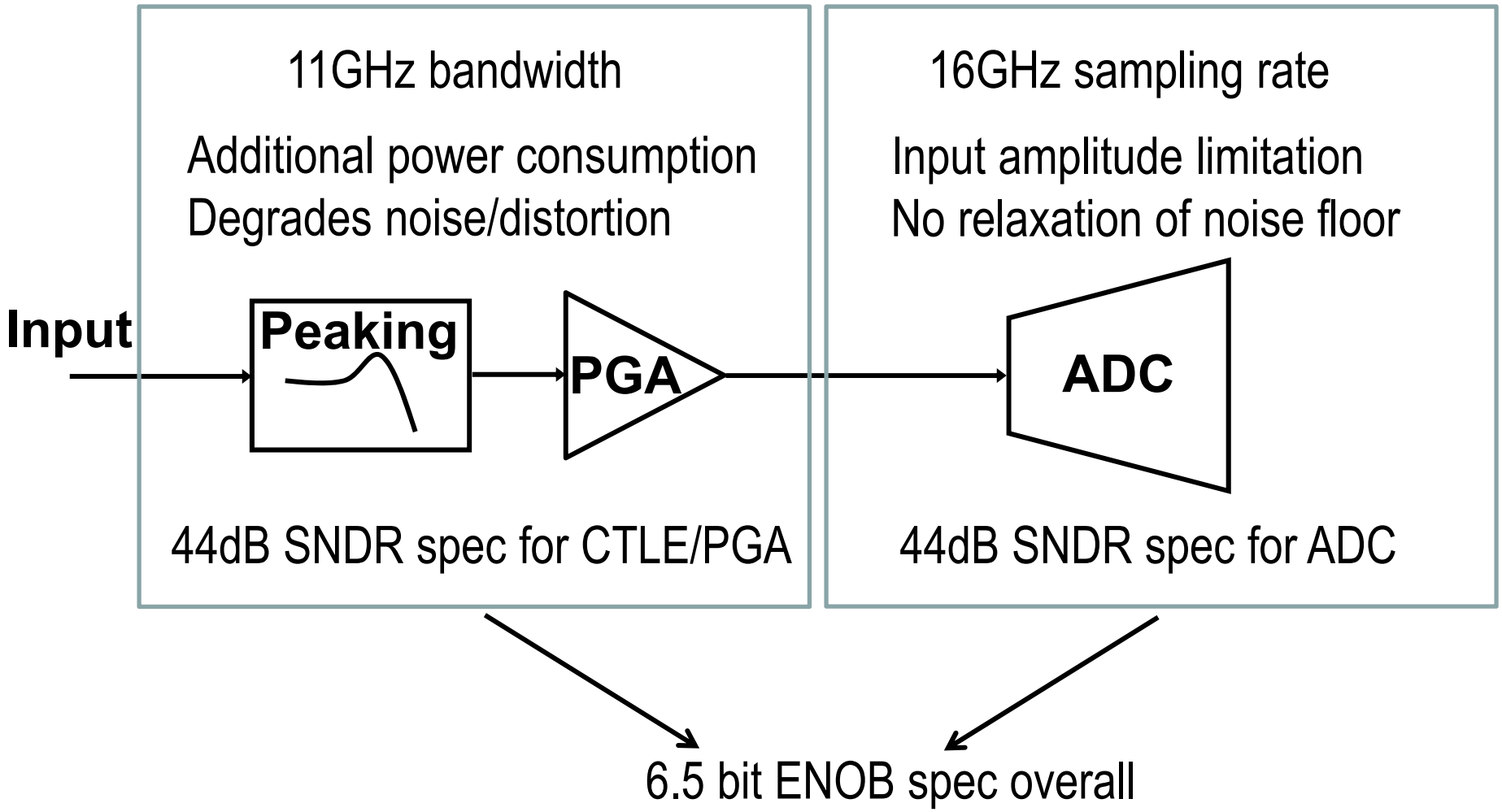
- High speed ADC (>10Gbps) requires time-interleaving
  - Significant loading to the input
  - A 1pF cap introduces a pole at 3.2GHz (50ohm)
  - ADC loading varies with input signal amplitude

ADC Based Solution with CTLE/PGA

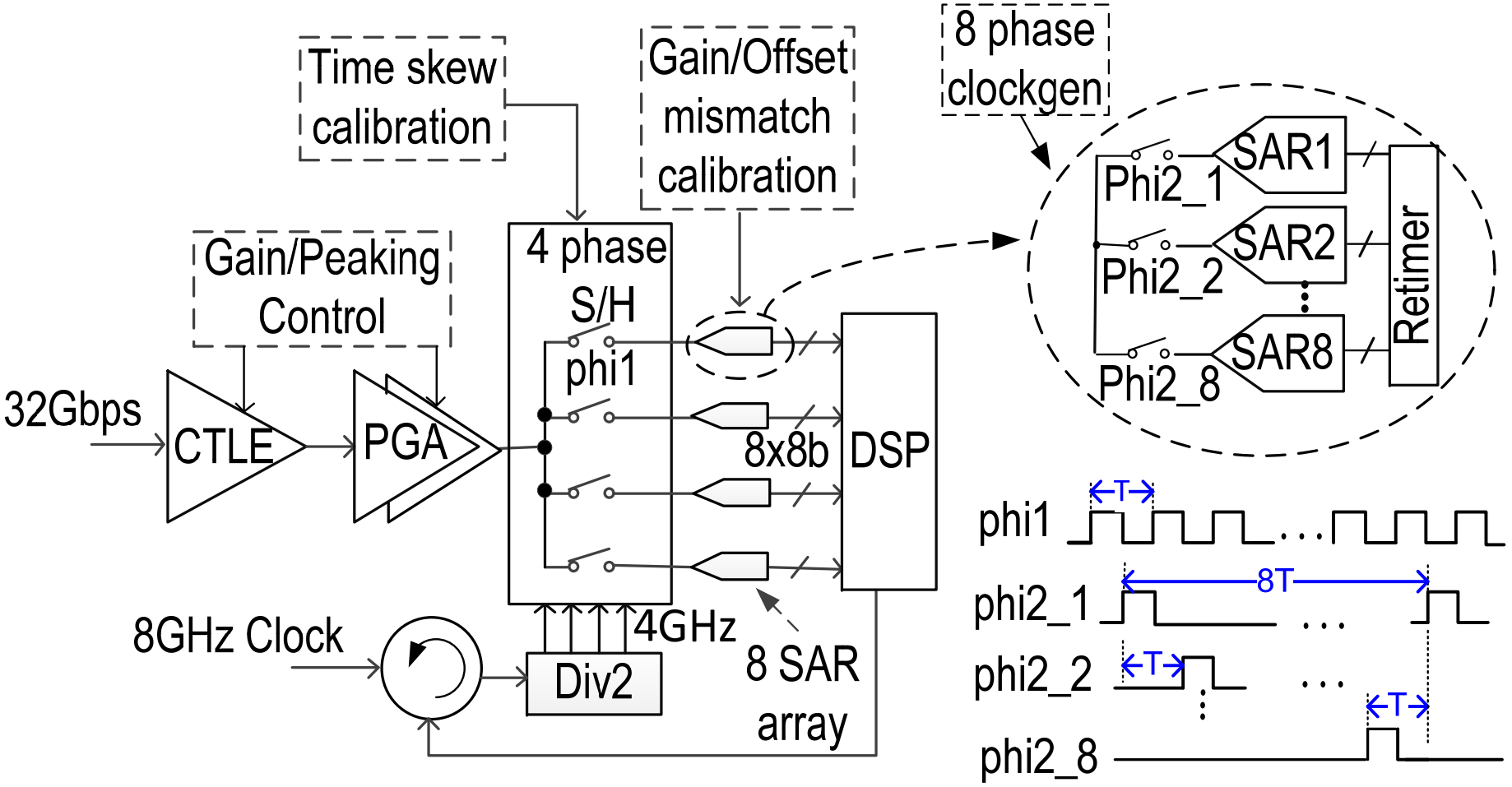


- ADC preceding by CTLE/PGA stage
  - Significantly lower loading capacitance
  - CTLE extend the loss compensation capability
  - PGA adapts the input amplitude variation

Noise/Distortion of CTLE/PGA



ADC-based Analog Front-End Architecture

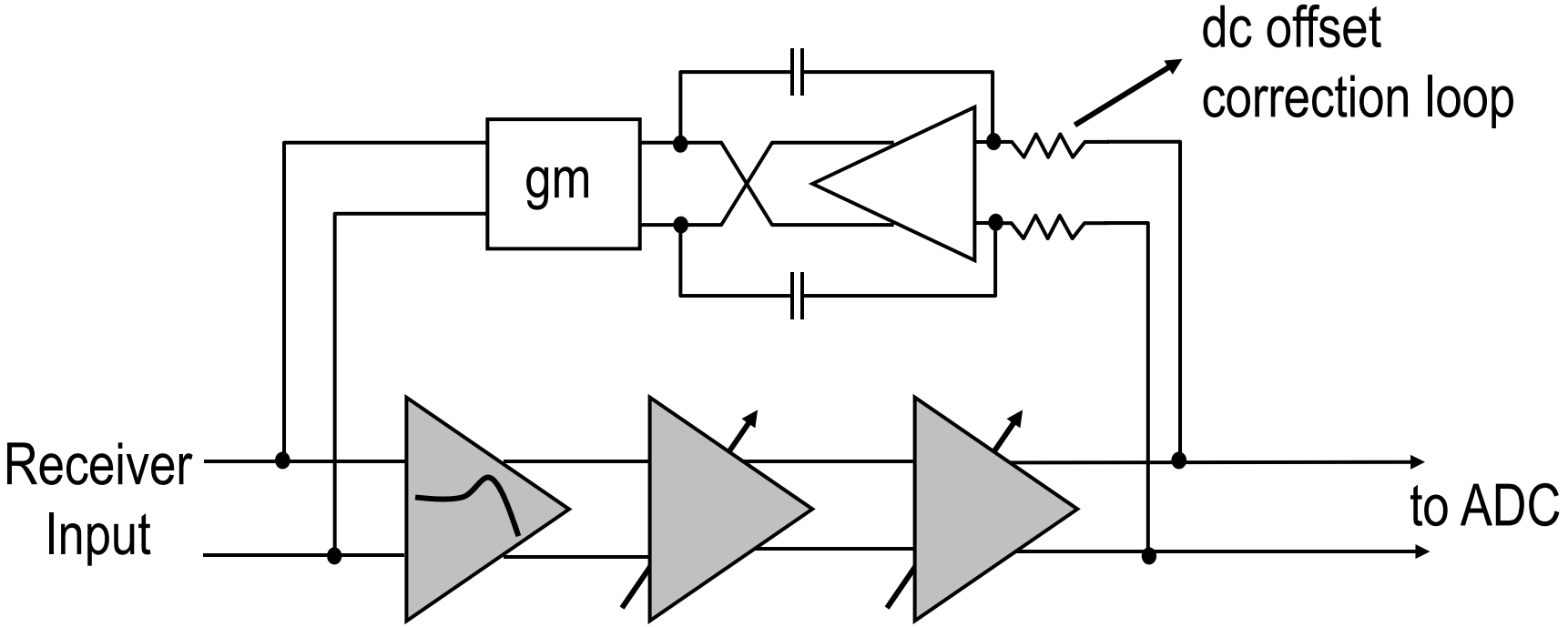


ADC interleaves 4×8×0.5GHz unit SAR ADC (16GHz sampling rate)

Outline

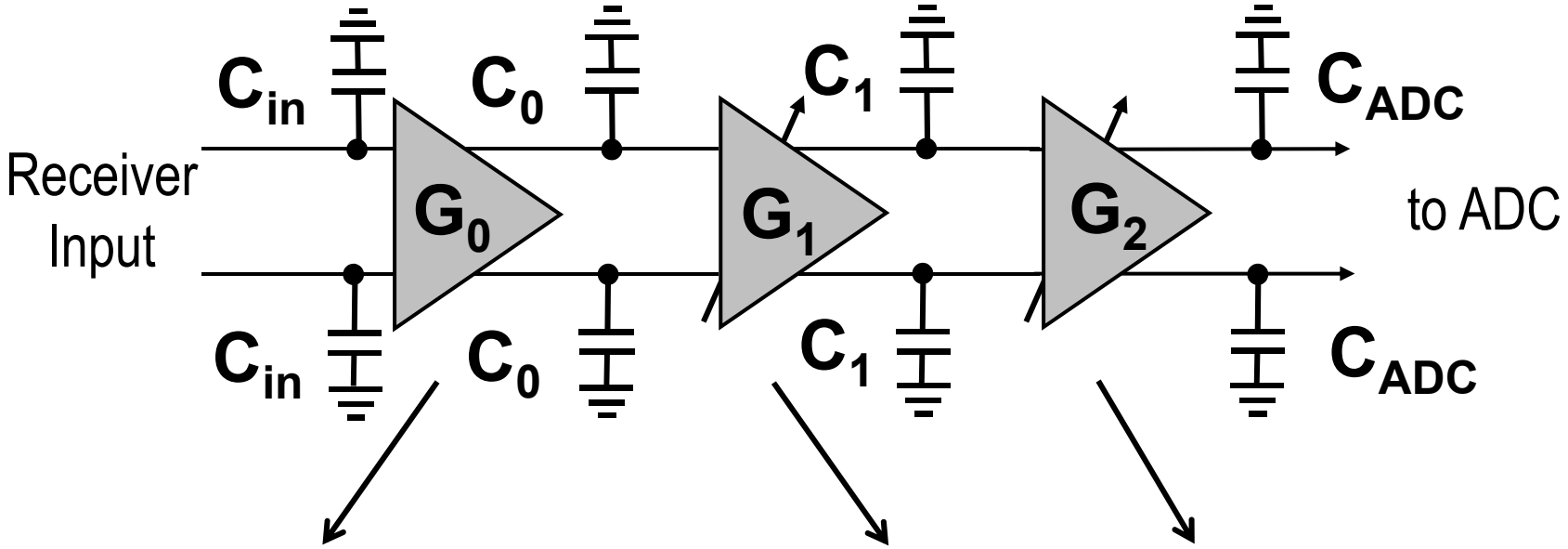
- Introduction
- ADC-based Analog Front-End Architecture
- ***Circuit Implementation***
- Measurement Results
- Comparison and Summary

CTLE/PGA



Gain Range	>14 dB
Bandwidth	>11 GHz
Peaking	7 dB
SNDR	43.5 dB
Output DC Offset	<1 mV

Low Noise/THD of CTLE/PGA

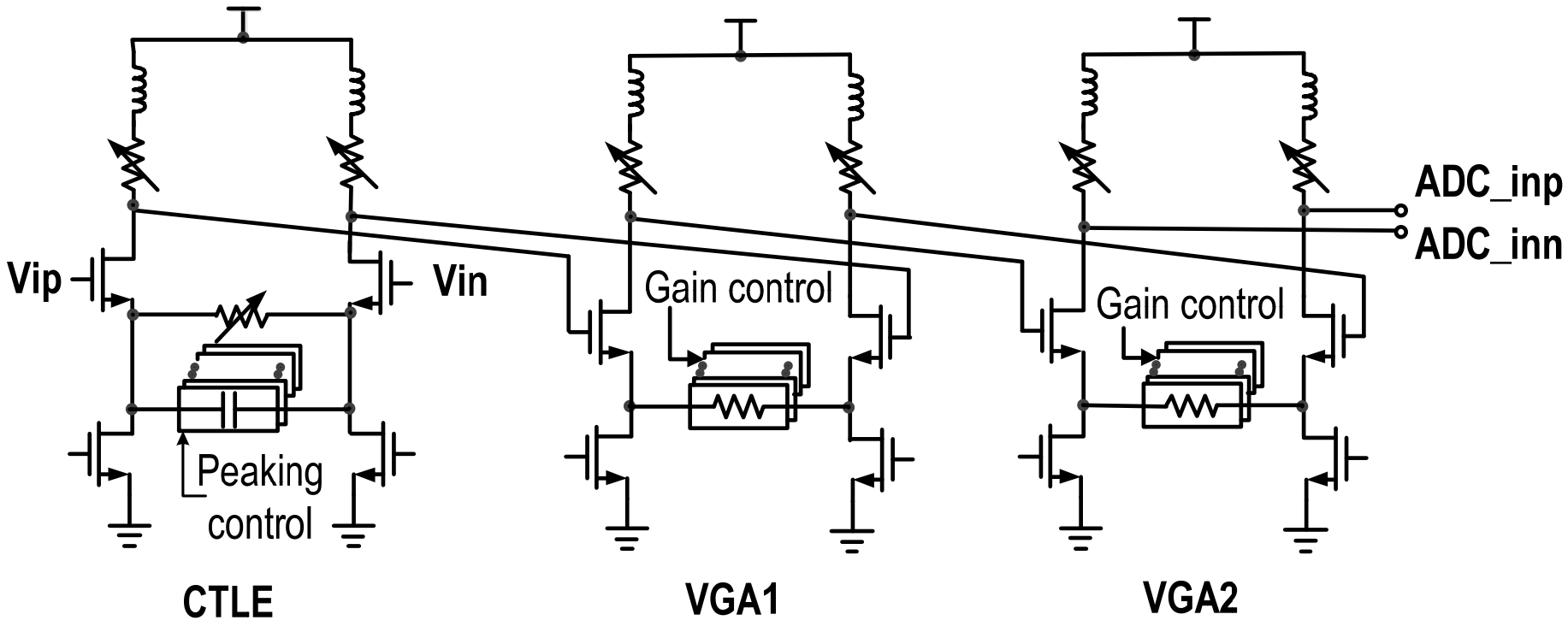


CTLE as first stage due to the DC loss in peaking mode

Optimum Gain distribution

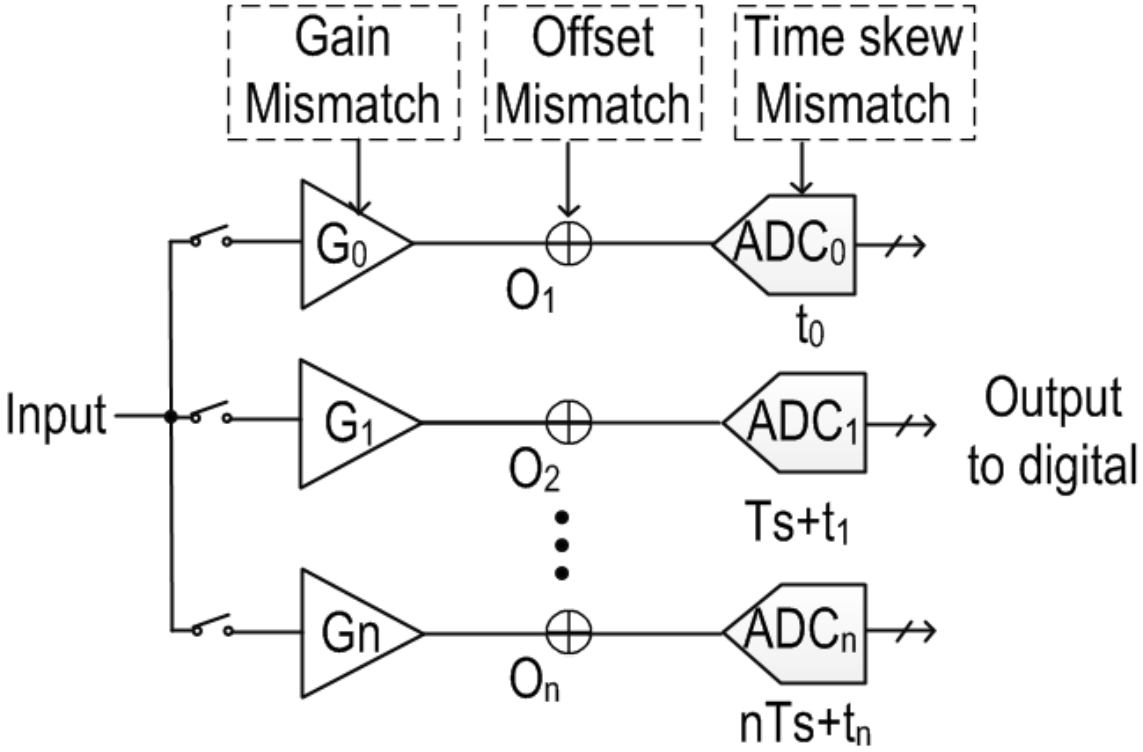
- Noise/THD tradeoff
- Noise/Bandwidth tradeoff

CTLE/PGA Circuit Schematic



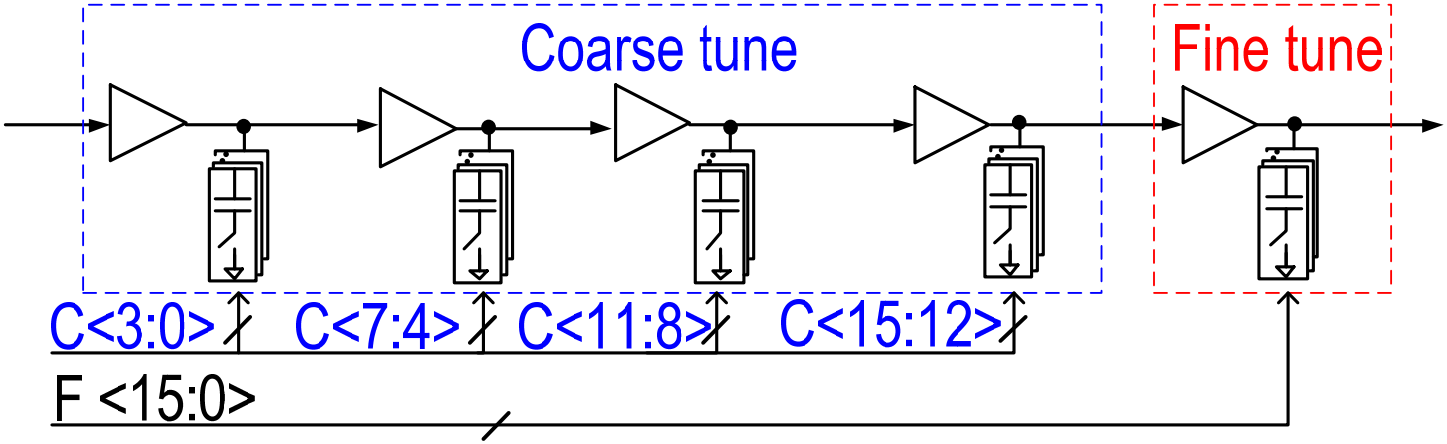
- CTLE + 2 stages of PGA
  - Capacitor DAC for peaking control adaptation
  - Resistor DAC for gain control adaptation
  - Shunt inductors are used for bandwidth extension
  - Calibrated load resistor for process adaptation

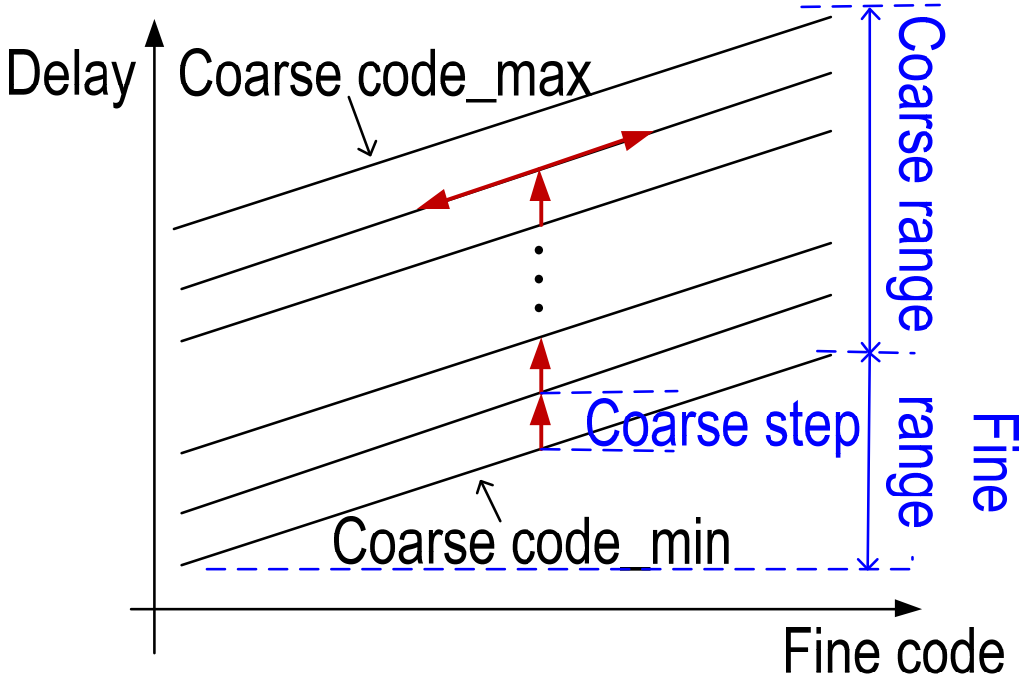
ADC Calibration



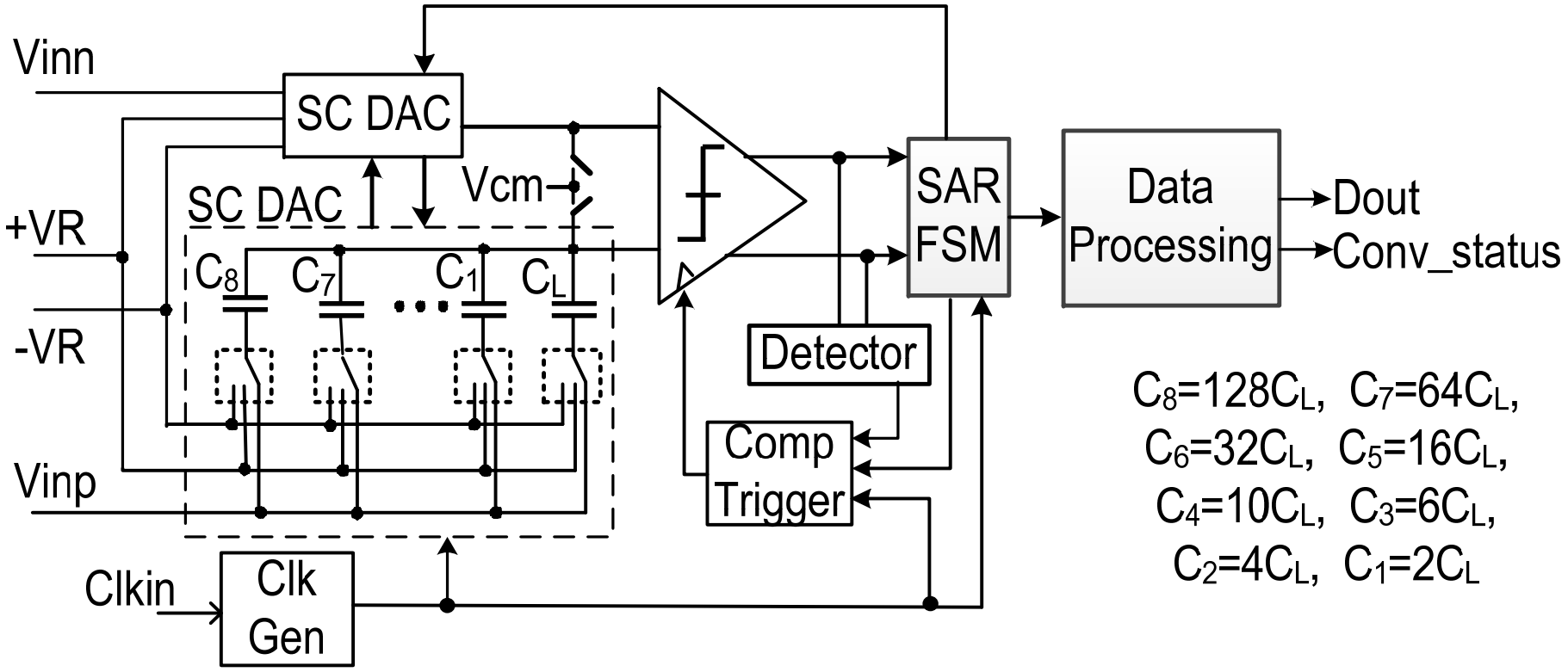
- Analog offset calibration is built in the comparator
- Digital calibration loop cancels gain mismatch
- A coarse-fine two step analog calibration approach is used to cancel time-skew mismatch

Time Skew Calibration



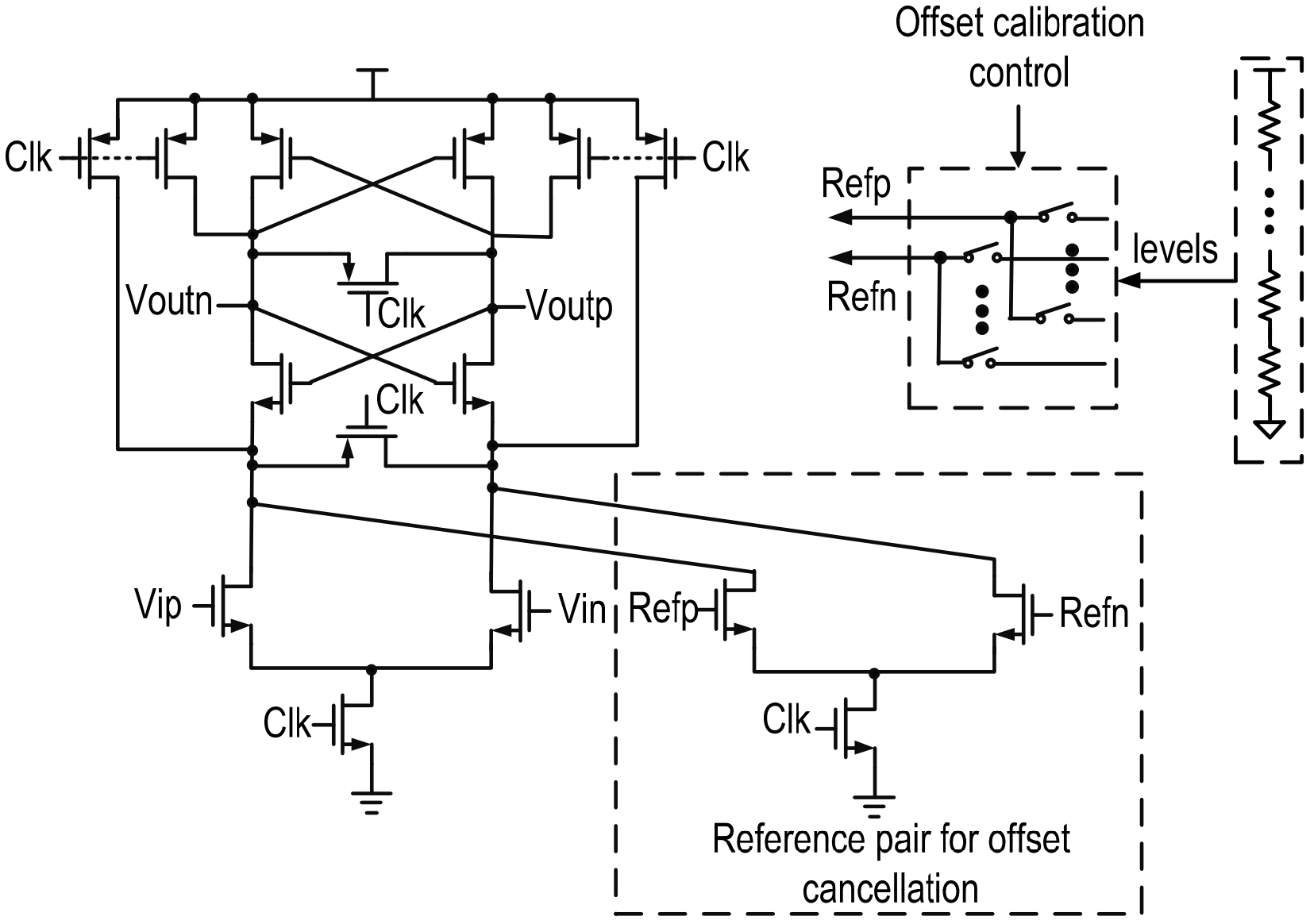


Unit SAR ADC

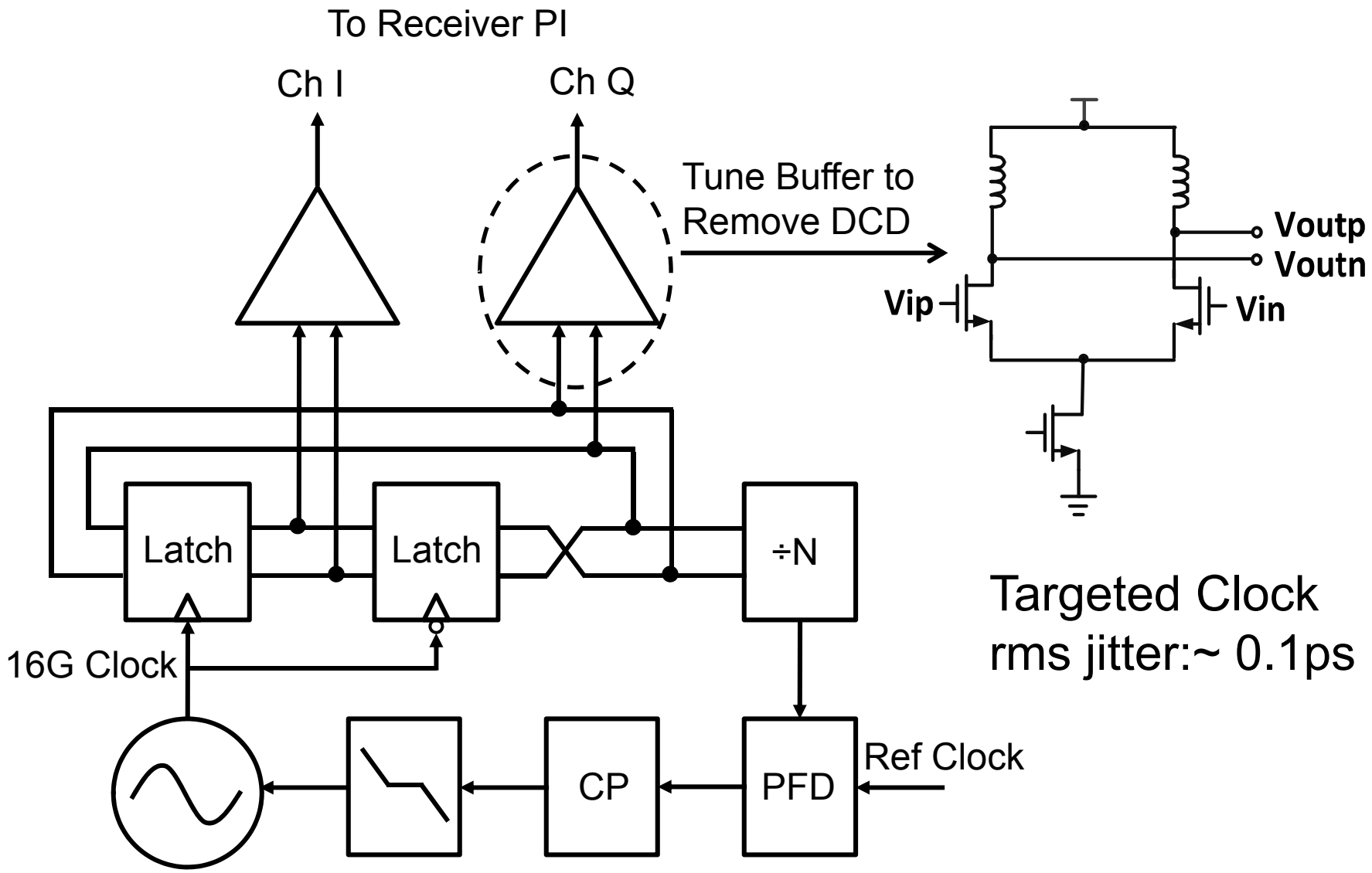


- 500MHz asynchronous unit SAR ADC
  - Sub-radix 2 DAC to provide over-range protection
  - Allow incomplete settling to maximize the speed

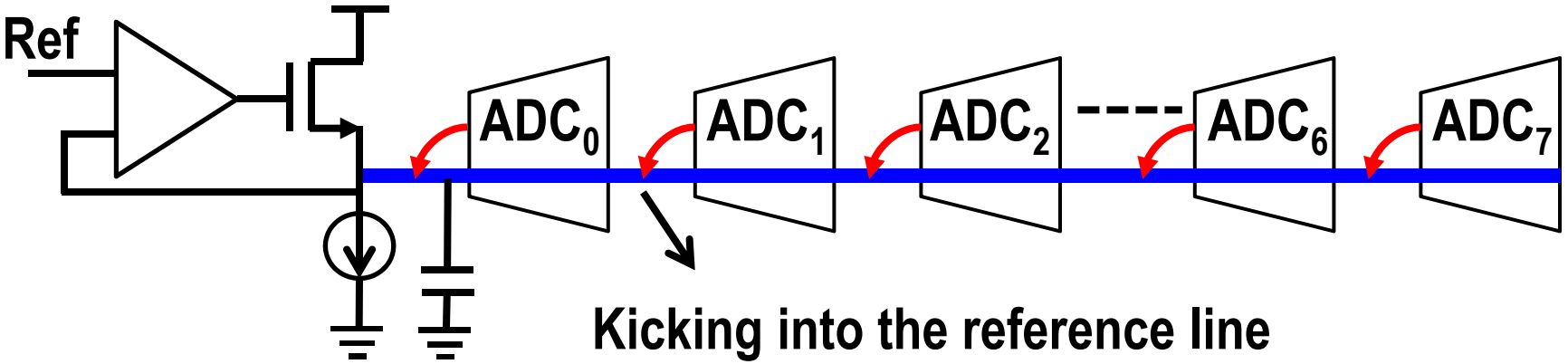
Comparator with Offset Calibration



Clock Generation/Phase Locked Loop



On Chip Reference Generation

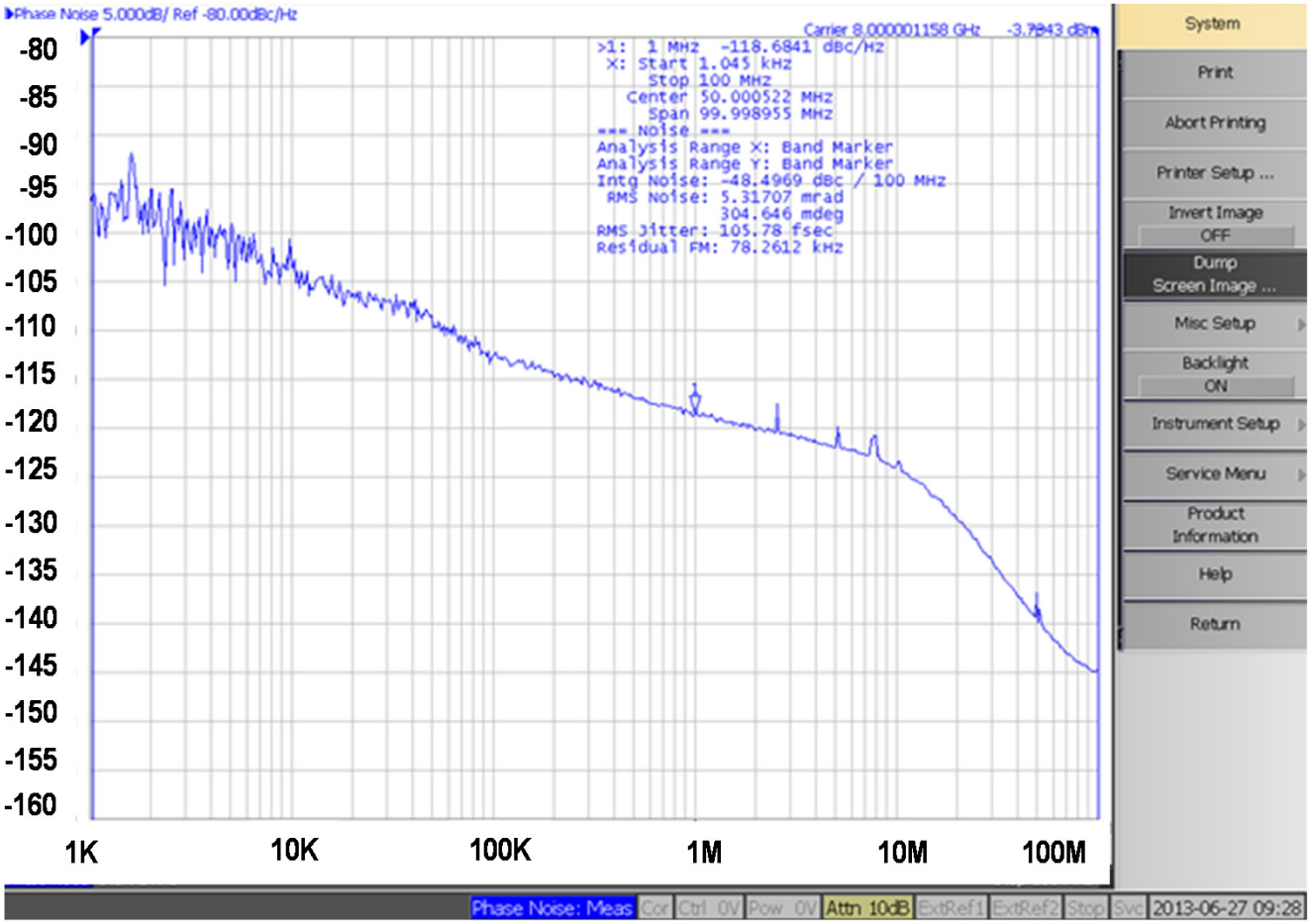


- One reference buffer driving 8 Unit ADC for better matching and to save power and area
  - DAC switching disturbs the reference voltage
    - Reference distribution line maintains low impedance
    - Over-range protection relaxes the current/cap requirement of the reference buffer

Outline

- Introduction
- ADC-based Analog Front-End Architecture
- Circuit Implementation
- ***Measurement Results***
- Comparison and Summary

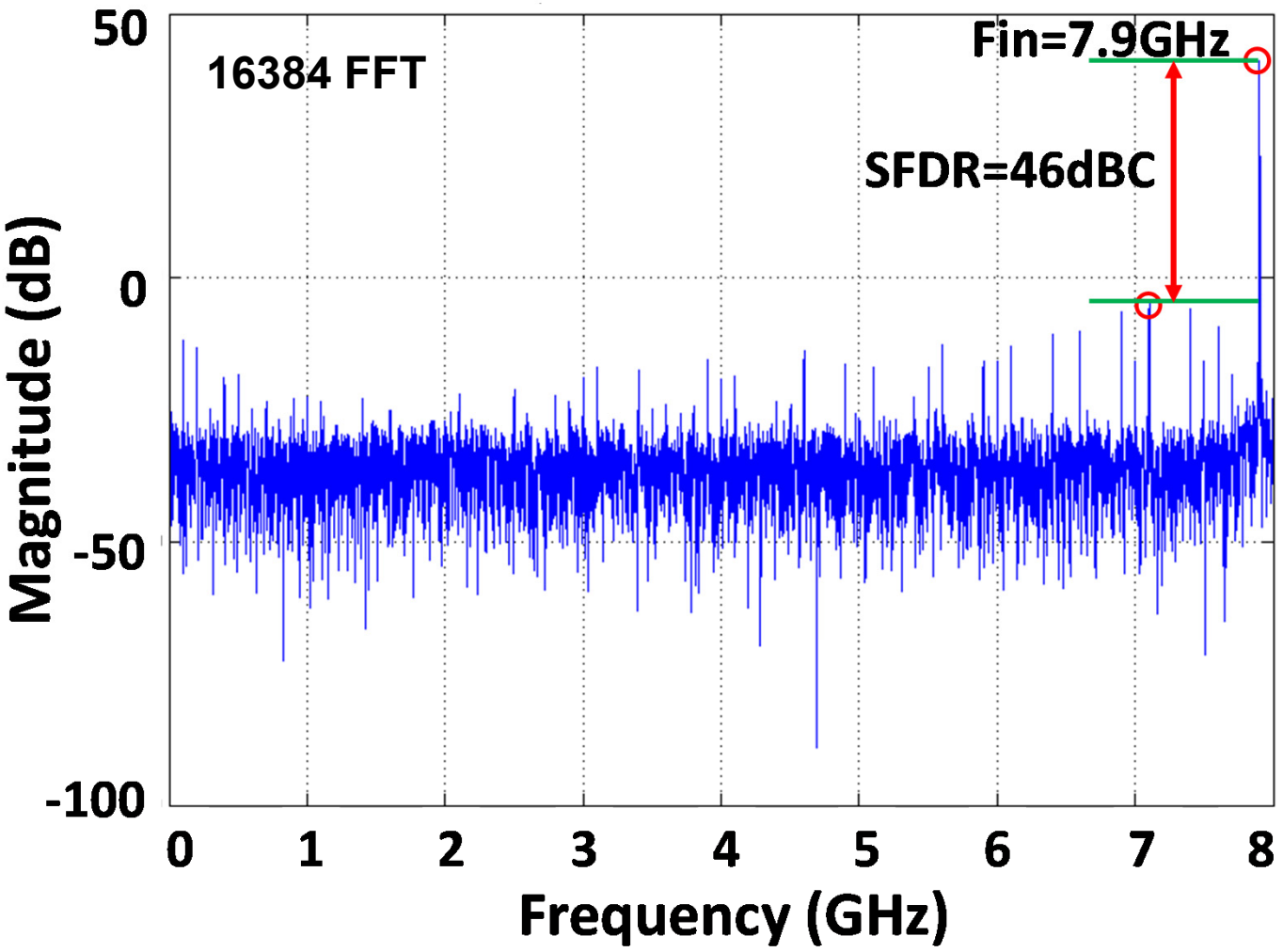
Measured PLL Output Clock Spectrum



Measured Phase Noise: 0.106ps, integration:1KHz to 100MHz

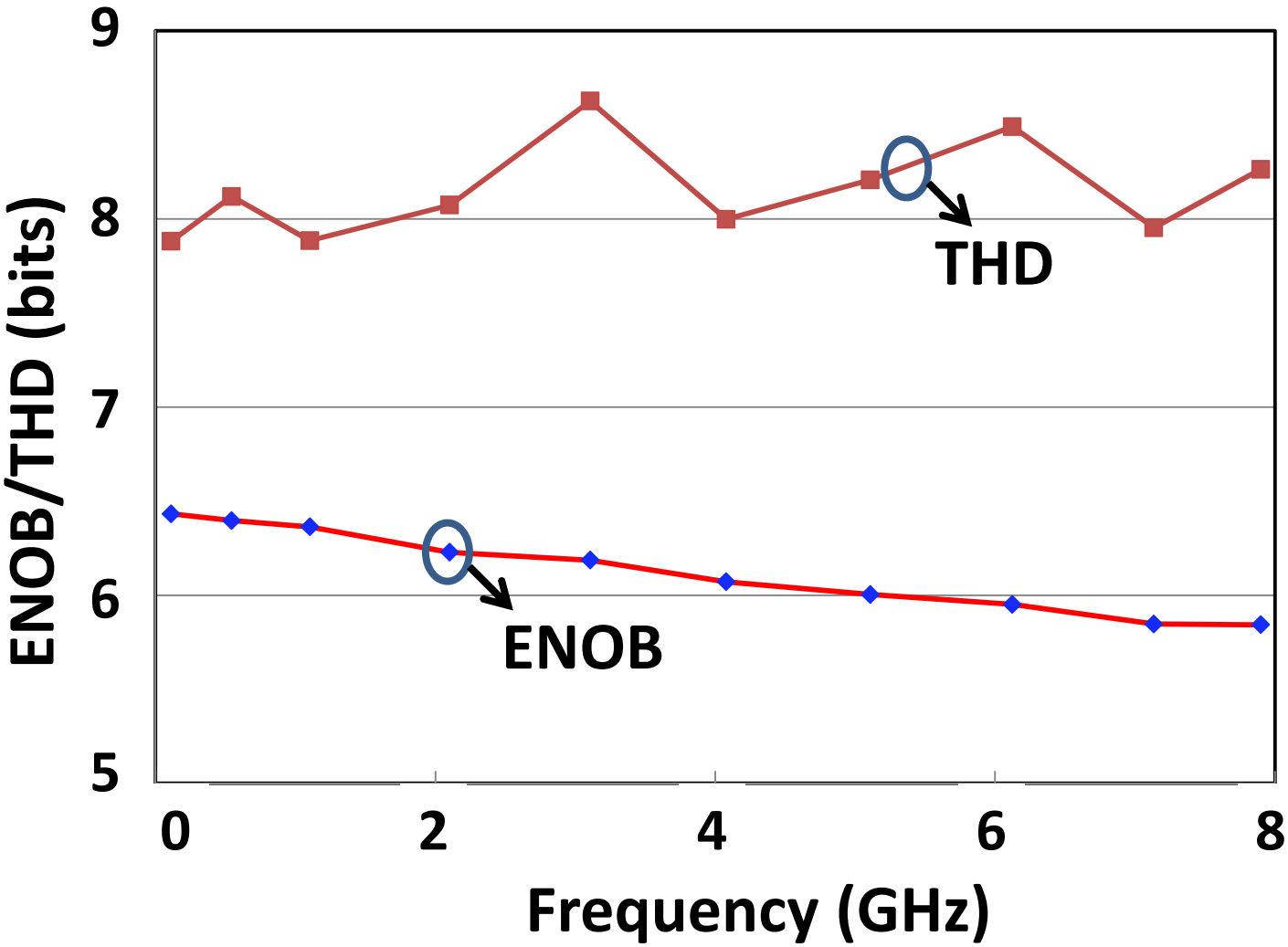
Phase Noise: -118dBc/Hz at 1MHz

Measured ADC Spectrum at Nyquist



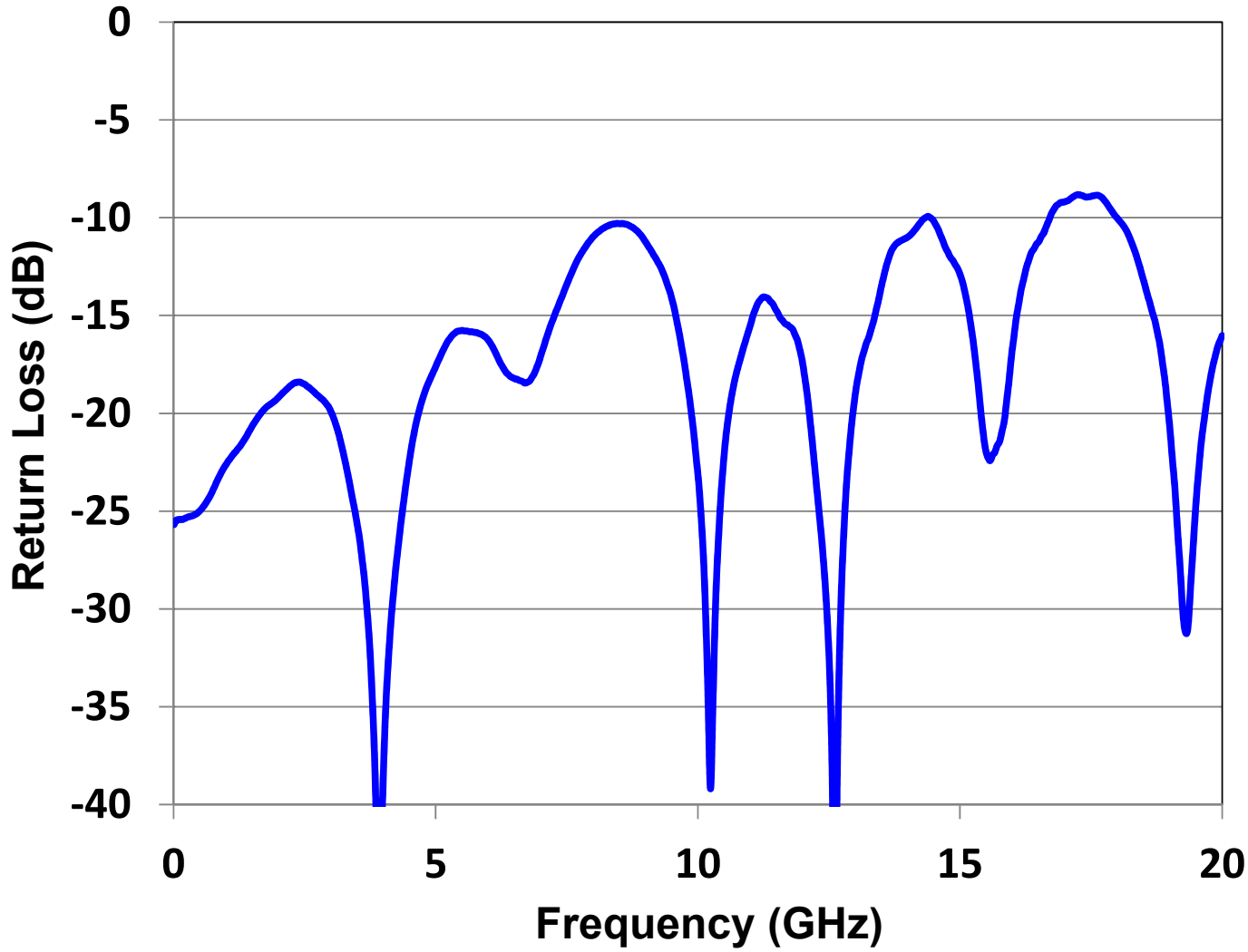
Sampling Frequency: 16GHz, SFDR=46dBc, ENOB=5.85bits

AFE ENOB versus Frequency



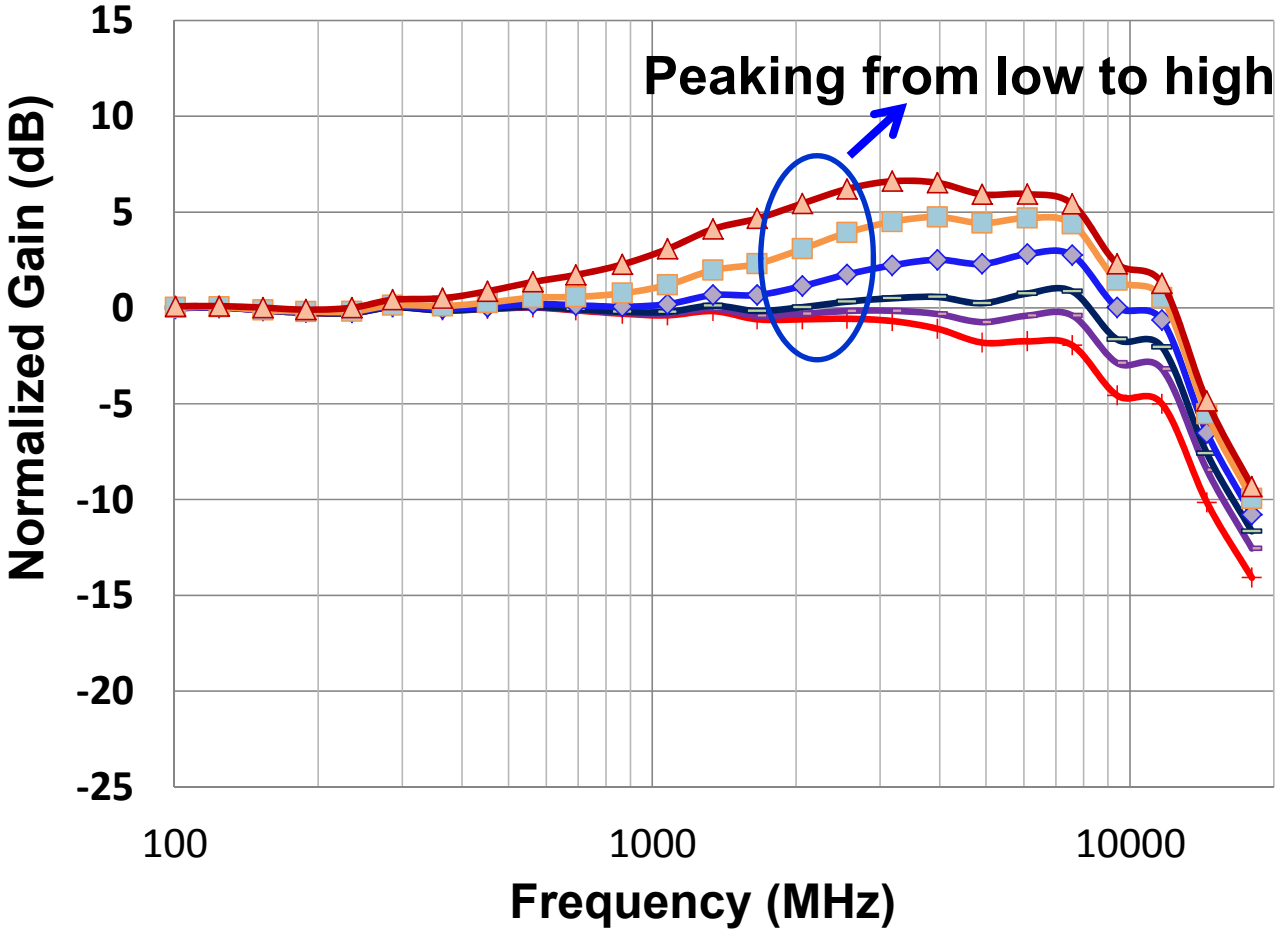
ENOB: 6.4 bits at DC and 5.85 bits at Nyquist

Return Loss Measurement



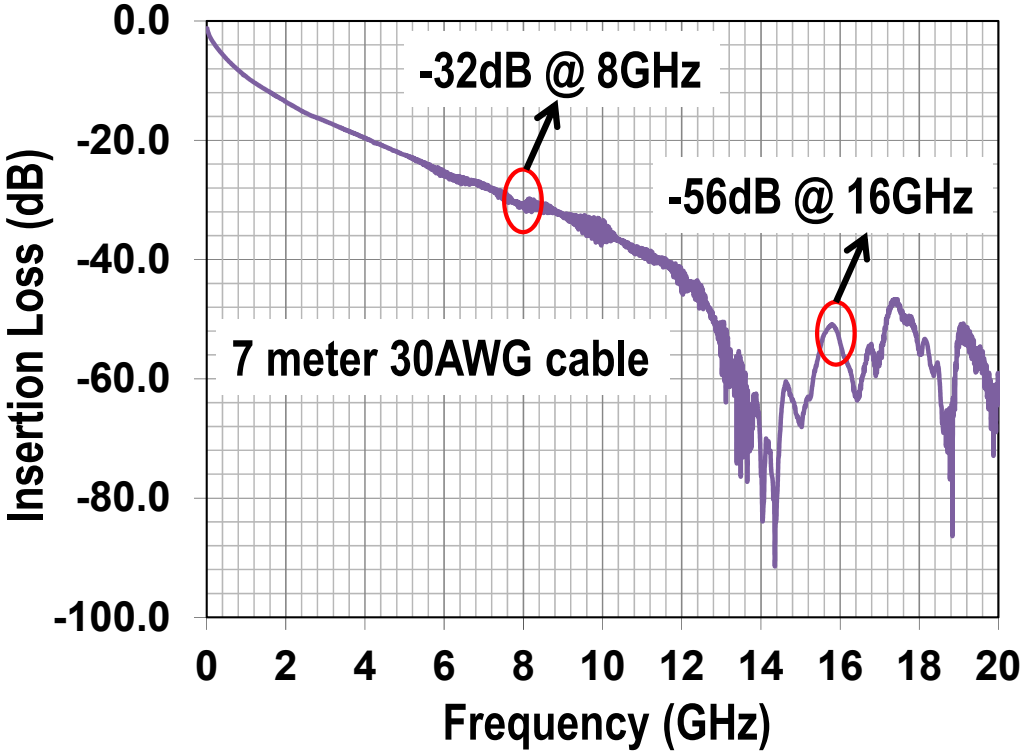
Differential return loss less than -10dB up to 16GHz

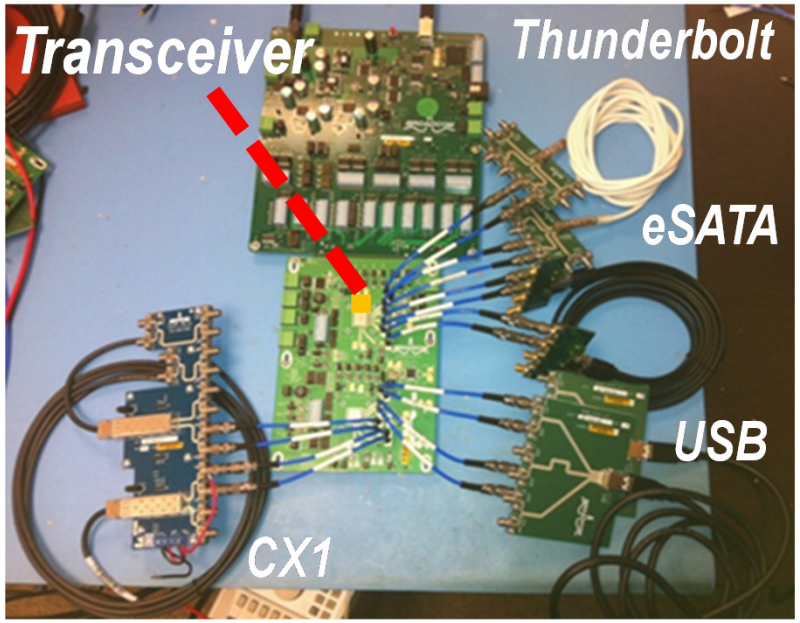
Bandwidth and Peaking



Bandwidth > 11GHz and Peaking Range > 7dB
Measurement with ~1dB additional board loss at 10GHz

Measurement Setup

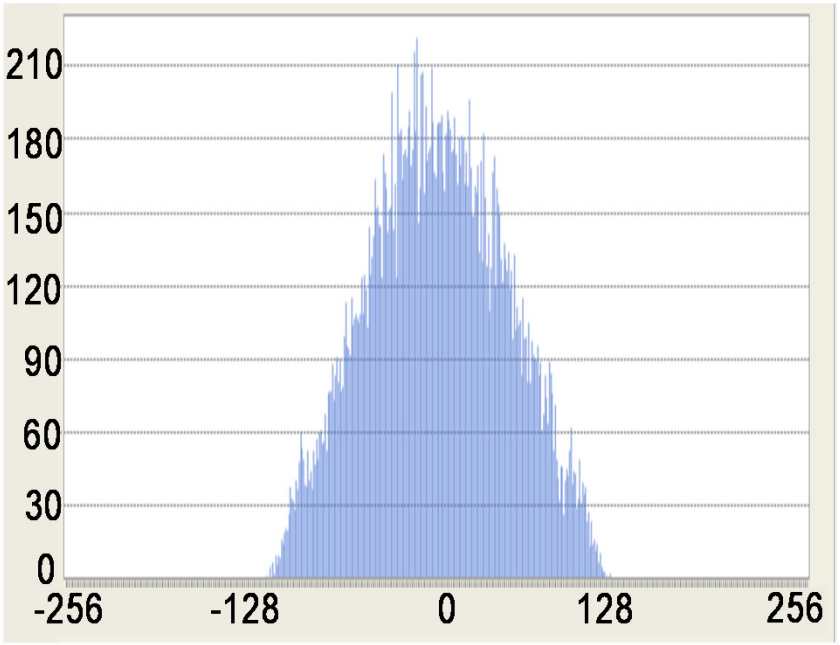


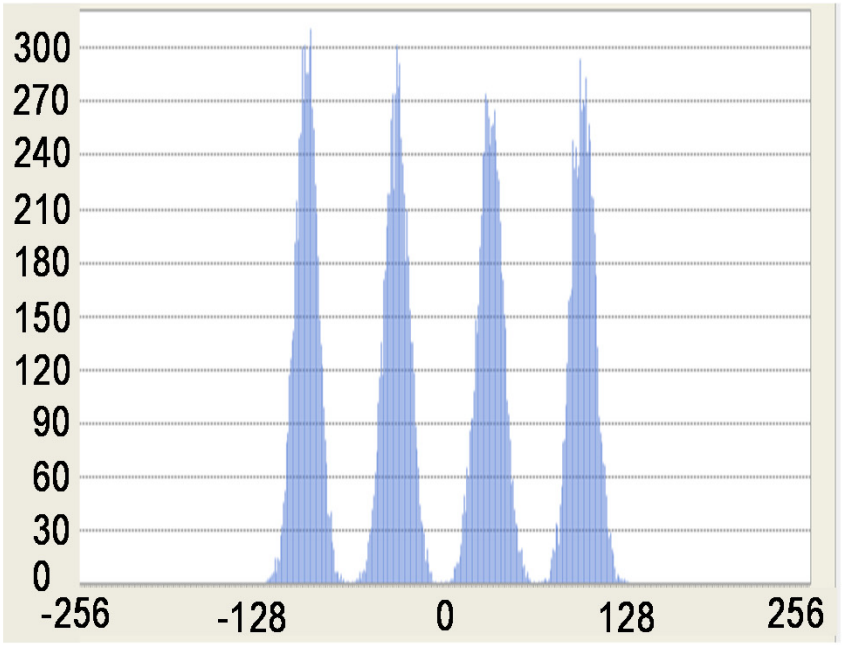


- Measurement has been performed with
  - Various backplane and cables
  - Low cost medium channels: eSATA, CX1 and USB
  - BER free operation with channel loss up to 32dB at 8GHz

Channel Equalization

Histogram of the Recovered Eye

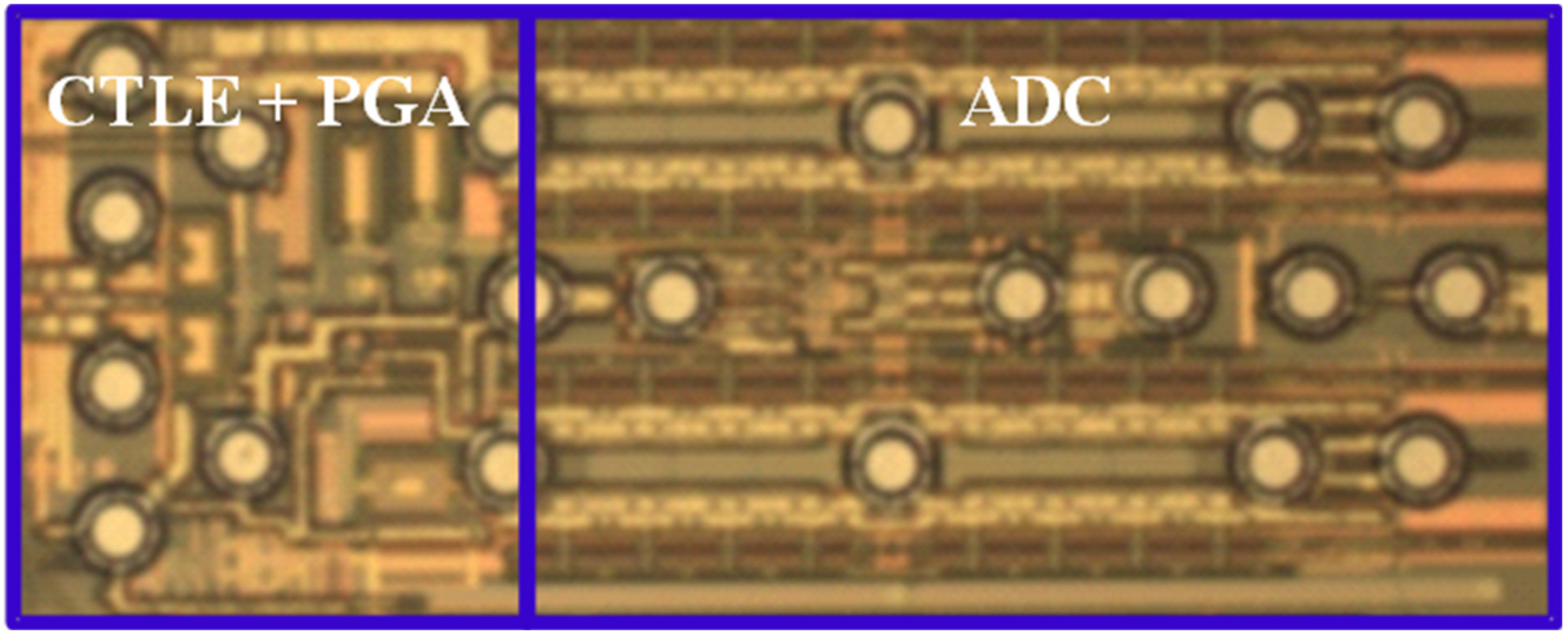




Before Equalization

After Equalization

Chip Photo



- Chip fabricated in 28nm CMOS
- Analog front end area is 0.89mm^2
- Chip consumes 320mW
  - Including ADC, CTLE/VGA, Clock and reference

Performance Summary

Process Technology	28nm CMOS
Power Supply Voltage	1.0V, 1.5V (For PGA)
Input Amplitude	375mV to 800mV
Sampling Frequency	16 GHz
Nominal resolution	8 Bits
Gain Adjustment	14 dB
Peaking Adjustment	0 - 7 dB
Bandwidth	11 GHz
ENOB at DC	6.4 bits
ENOB at Nyquist	5.85 bits
Clock Jitter (rms)	106 fs
Chip area	0.89 mm^2
Power Consumption	320 mW

Performance Comparison

Design	Harwood ISSCC 07	Verma ISSCC 13	Zhang ISSCC 13	Huang VLSI 10	This work
Technology	65nm	40nm	40nm	65nm	28nm
Sampling Rate (GS/s)	12.5	10	10	16	16
Data Format	NRZ	NRZ	NRZ	N/A*	PAM4
Data rate (Gbps)	12.5	10	10	N/A	32
Resolution (bit)	4.5	6	6	6	8
Power (mW)	230	240	195	435*	320
ENOB @ DC	N/A	5.5	4.9	4.35	6.4
ENOB @ Nyquist	N/A	5.1	4.6	N/A	5.85
Compensated Channel Loss @ Nyquist	15dB	35dB	34dB	N/A*	>50dB
FOM (fJ/c-s)	N/A	700	832	2600	350

* ADC Only, No VGA/CTLE

Conclusion

- ADC-based PAM4 Receiver Analog Front End
  - *Input data path provides 14dB gain adjustment, 7dB peaking adjustment range and 11GHz bandwidth*
  - *16GHz ADC supporting 32Gbps PAM4 format*
  - *6.4 bit ENOB at DC and 5.85 bit ENOB at Nyquist*
  - *0.1ps rms clock jitter*
  - *320mW total power consumption*
  - *Compensating channel loss of up to 32dB at 8GHz*

Acknowledgement

The authors would like to thank the support of the Broadcom DSP, ASIC and Layout groups in AFE design and layout and the DVT groups for the measurement.

A 25-Gb/s Multi-standard Serial Link Transceiver for 50-dB Loss Copper Cable in 28-nm CMOS

Takayasu Norimatsu[1], Takashi Kawamoto[1], Kenji Kogo[1], Naohiro Kohmu[1], Fumio Yuki[1], Norio Nakajima[2], Takashi Muto[2], Junya Nasu[2], Takemasa Komori[2], Hideki Koba[2], Tatsunori Usugi[2], Tomofumi Hokari[2], Tsuneo Kawamata[2], Yuichi Ito[2], Seiichi Umai[2], Masatoshi Tsuge[2], Takeo Yamashita[2], Masatoshi Hasegawa[2], Keiichi Higeta[2]

[1]Hitachi Ltd., Tokyo, Japan

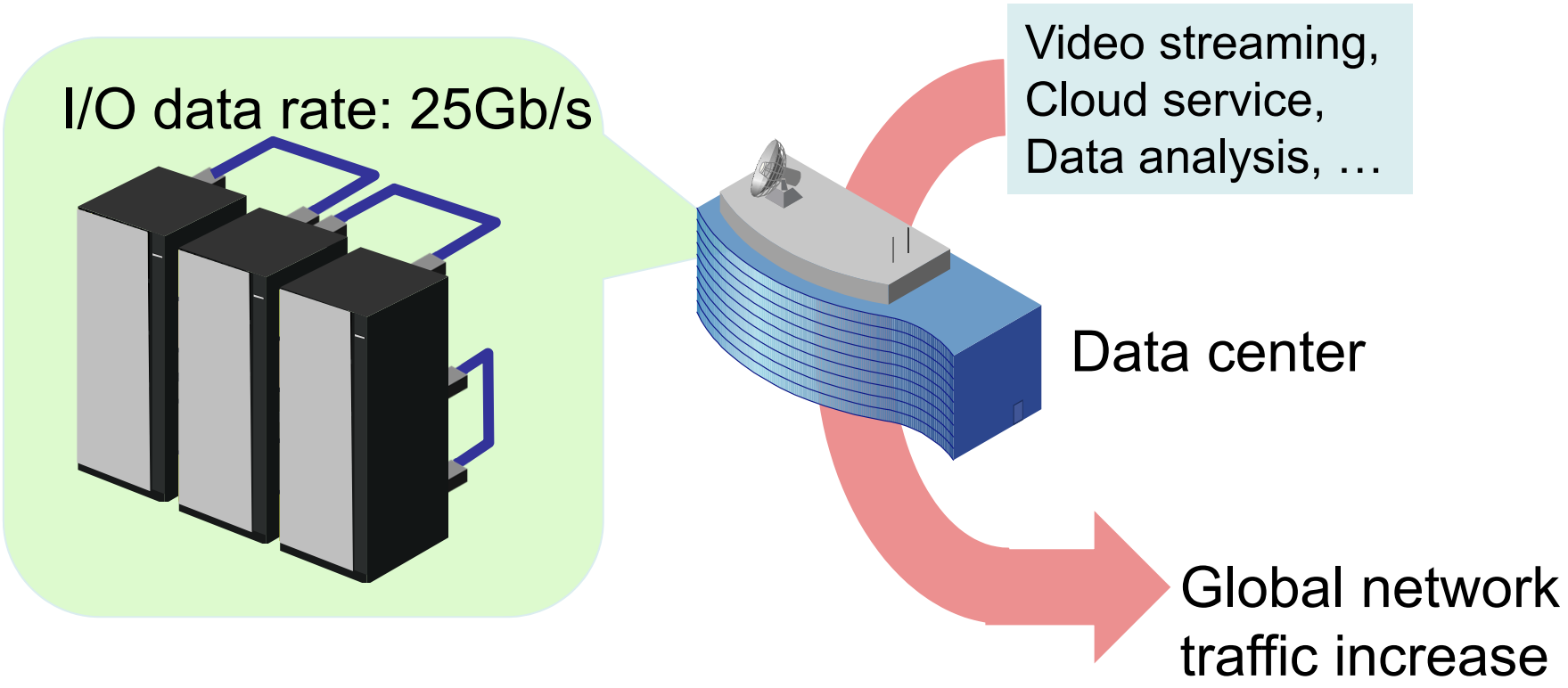
[2]Hitachi Ltd., Kanagawa, Japan

Contents

- Introduction
- Transceiver architecture
  - Proposed slicer in DFE
  - DC offset compensation
  - CTLE with low-frequency equalizer
- Evaluation results
- Conclusion

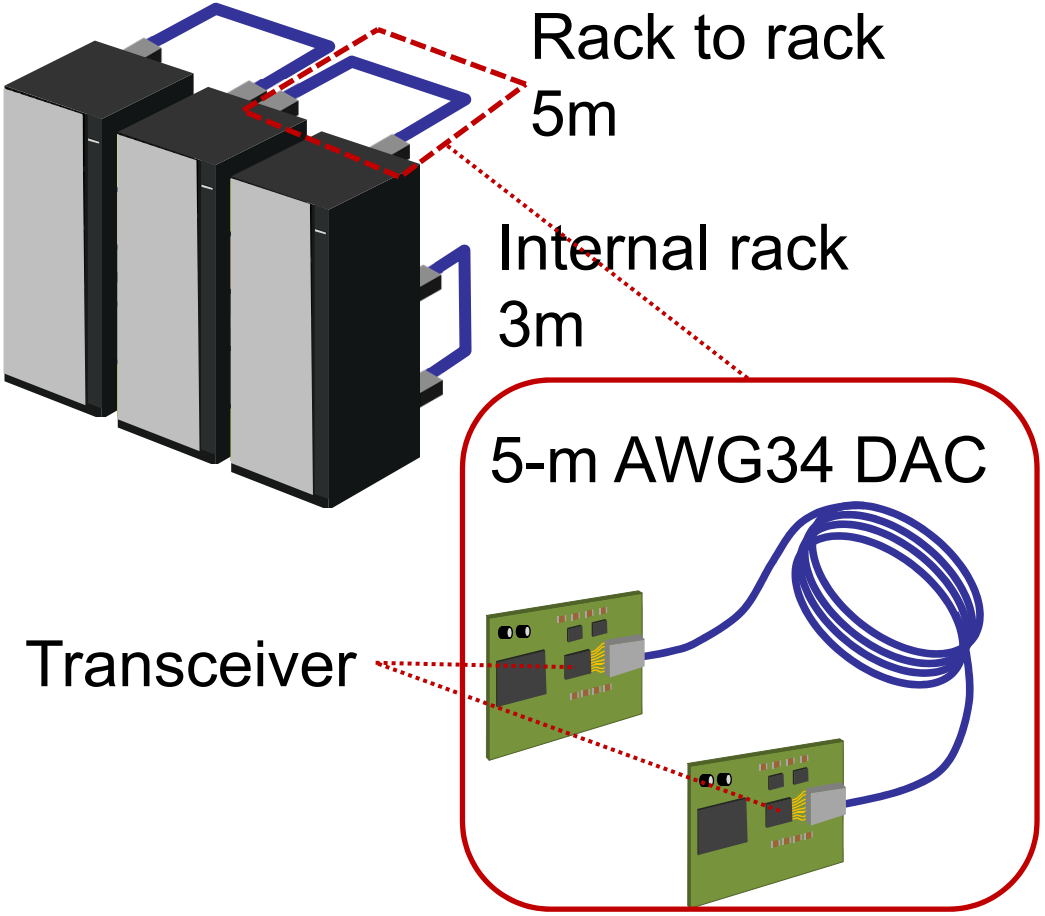
Background

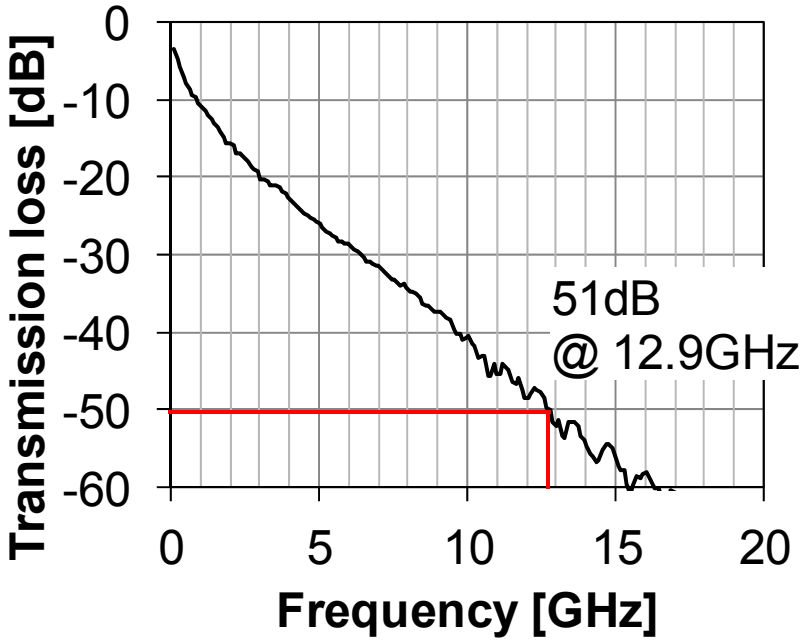
- Higher I/O data rate is demanded for data traffic growth in global network.



Motivation

- Large number of connections
  ➔Use a thinner and longer copper cable





Target

- Data rate per channel: 25Gb/s
- Transmission loss < 50 dB
  - Improve SNR at RX input
  - Reduce ISI with equalizers
- Power consumption < 3.5W in 8-lane operation

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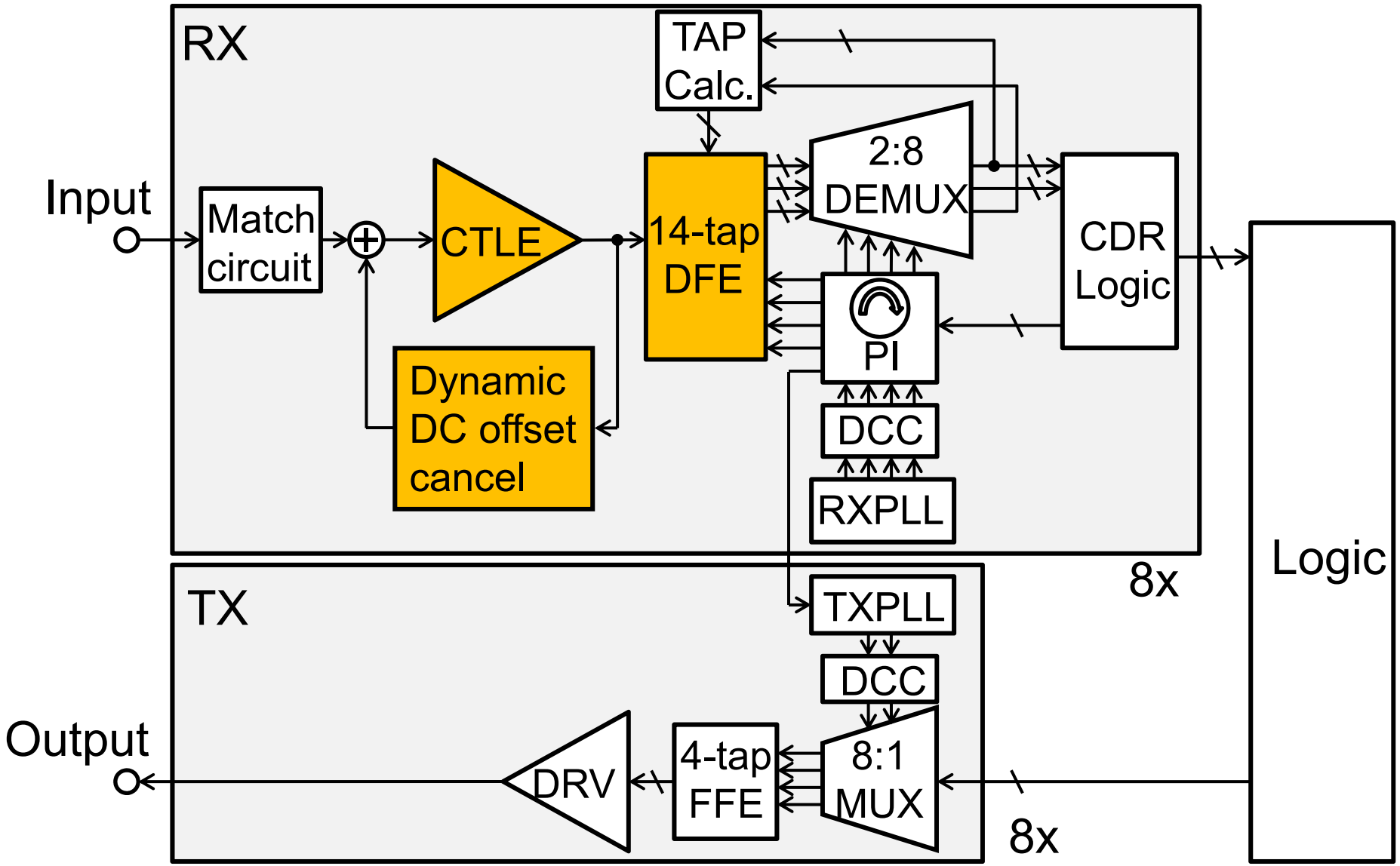
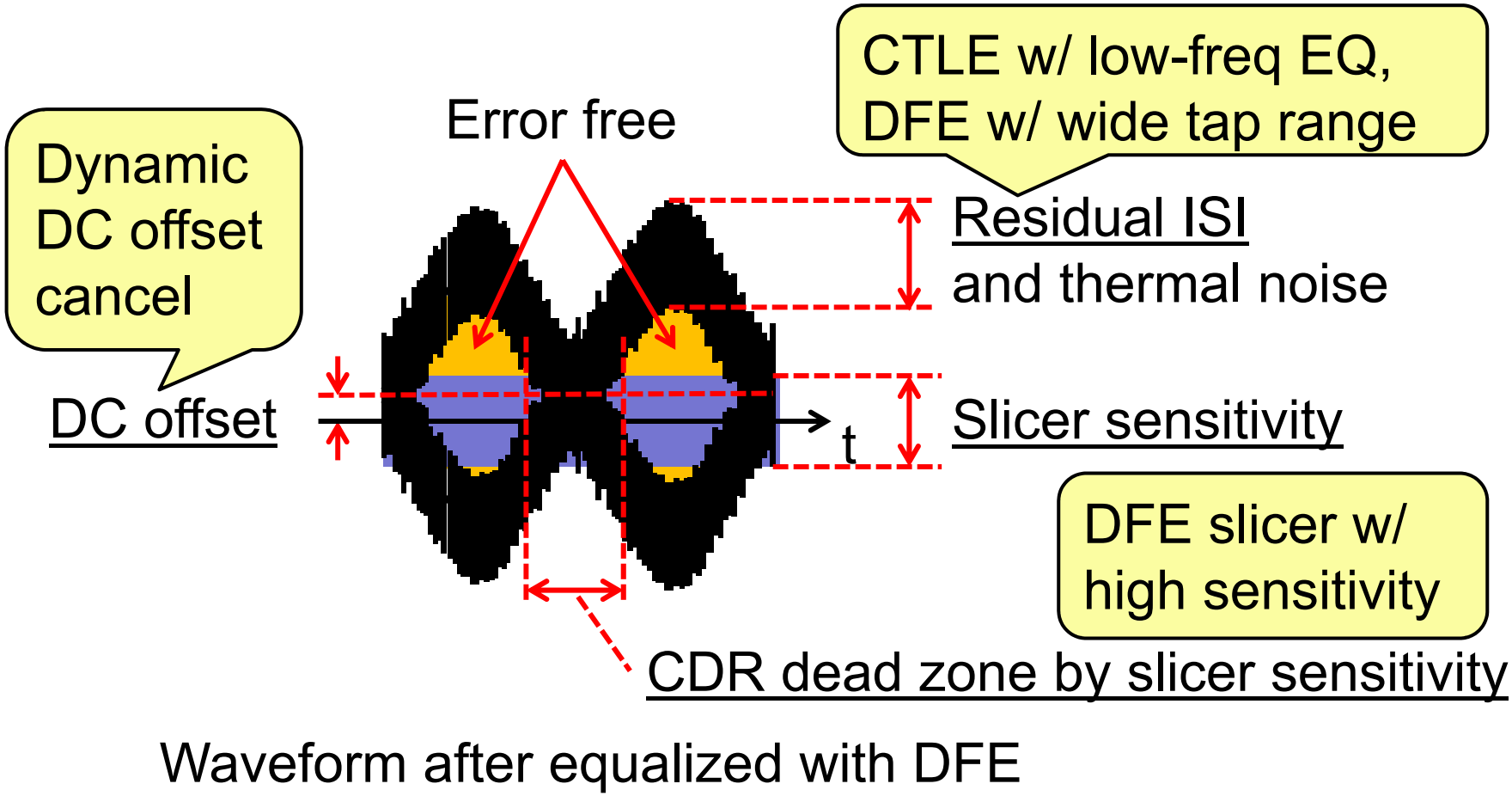
Transceiver architecture



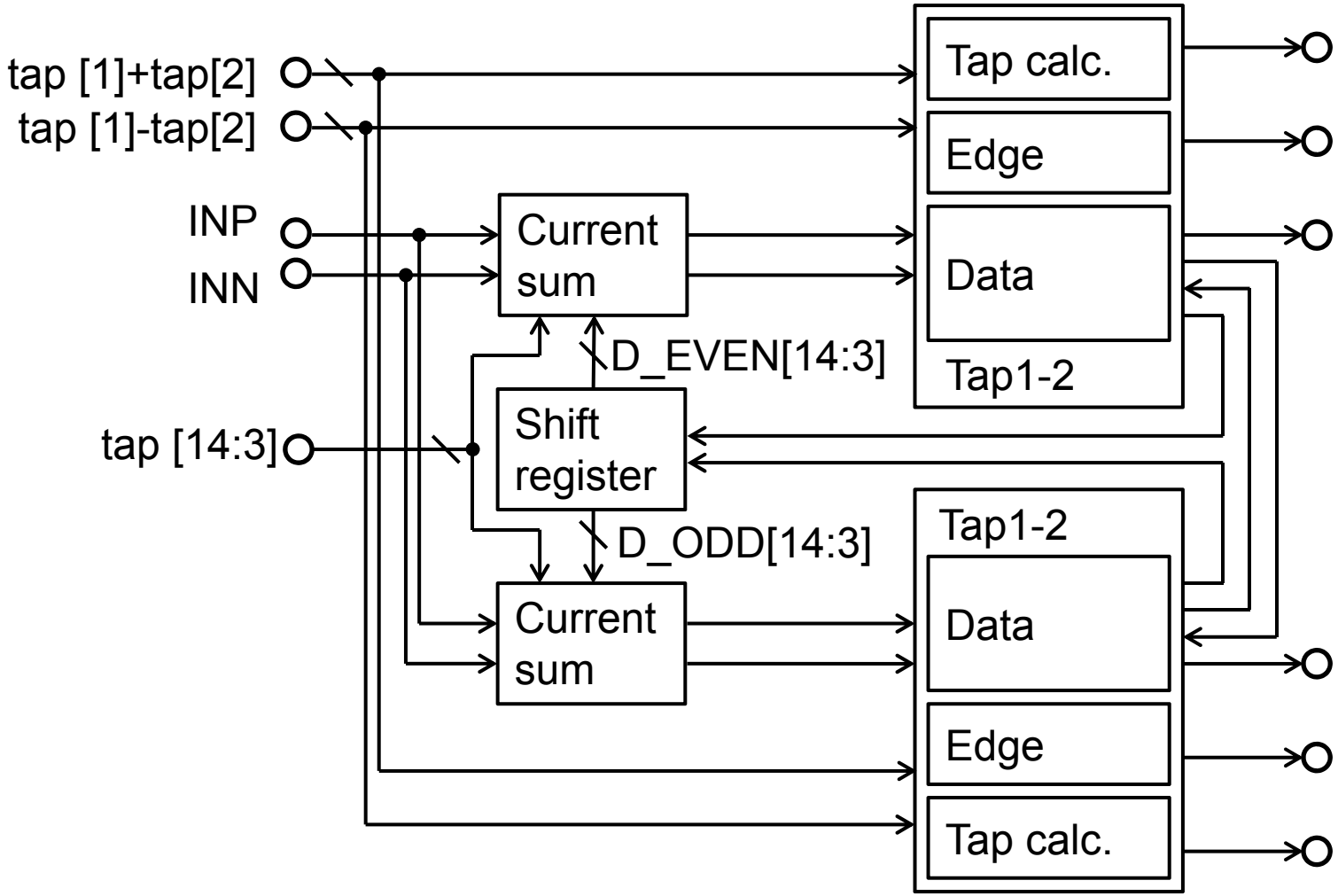
Issues in 50-dB loss data transmission

- Increase ratio of noise and ISI
- DC offset and slicer sensitivity reduce detection range



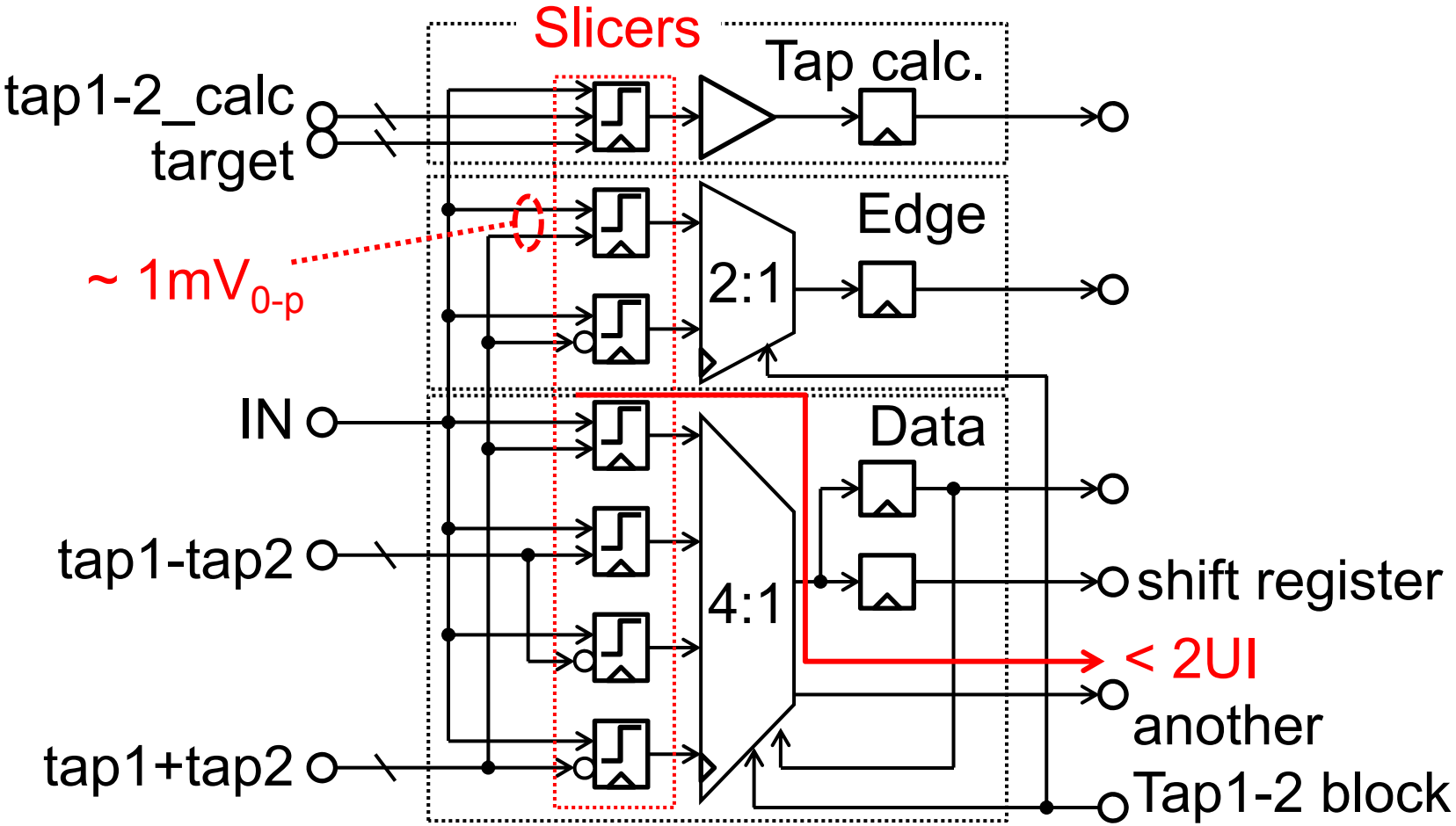
DFE architecture

- Half rate operation, 14 taps, 2-tap loop unrolled architecture



Tap1-2 block

- Satisfy delay requirements, reduce ISI
  ➔ Improve slicers

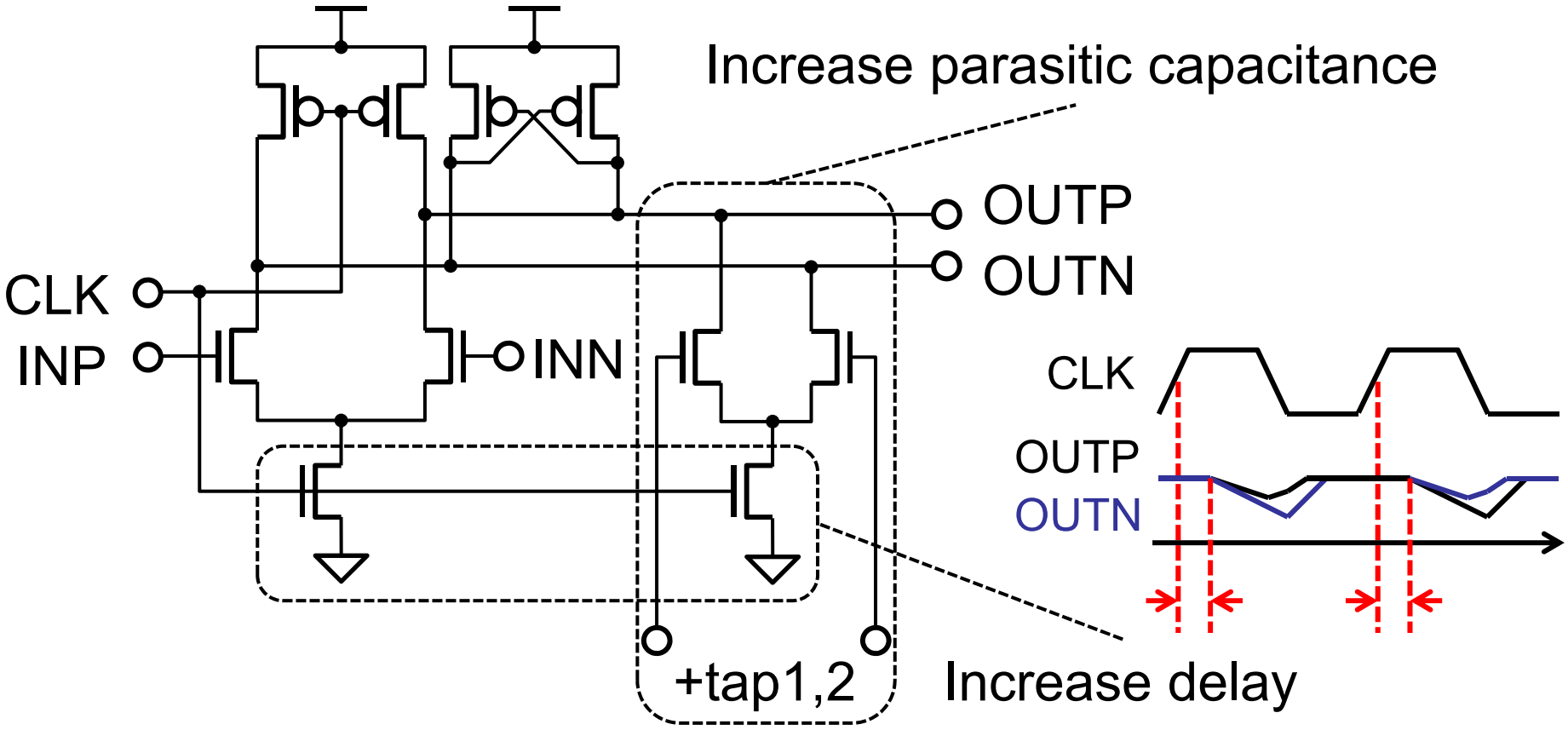


Slicer requirements

- Delay < 30ps
  - Achieve DFE delay requirements
- Minimum input sensitivity < $1.2mV_{0\text{-}p}$
  - Reduce CDR dead zone to 2ps
- Tap range > 60mV
  - 10-dB equalization gain with $100mV_{0\text{-}p}$ input

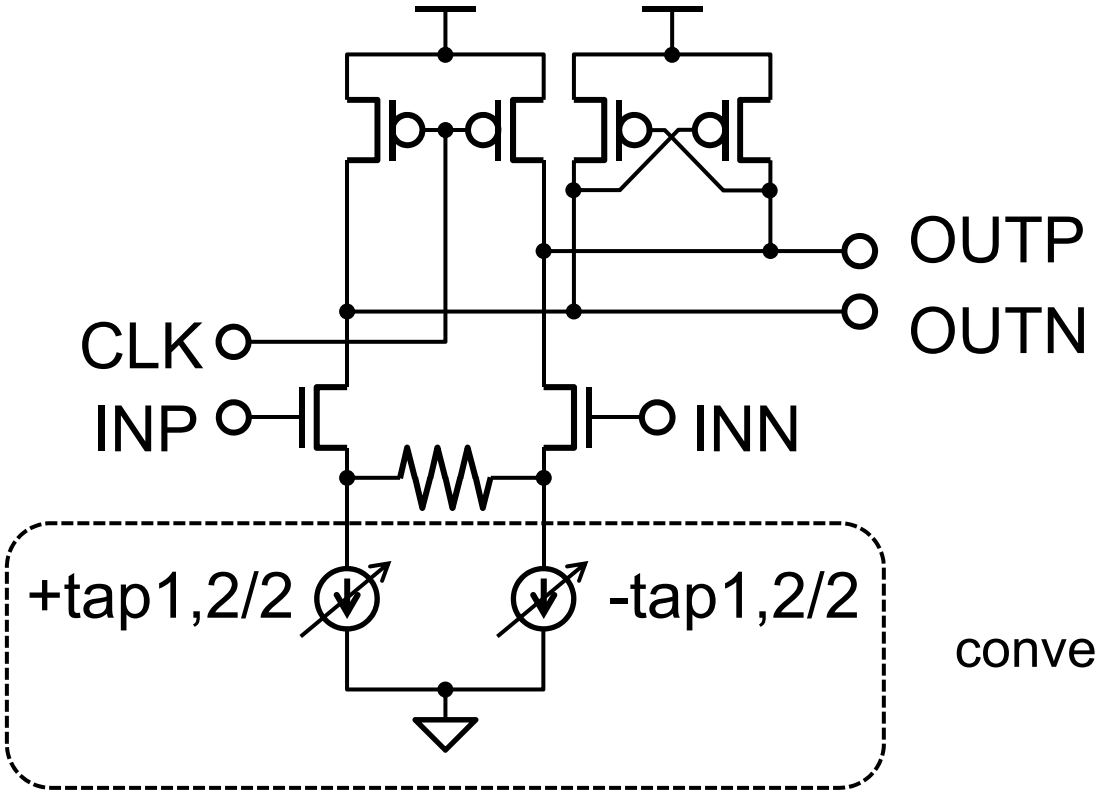
Example of a conventional DFE slicer

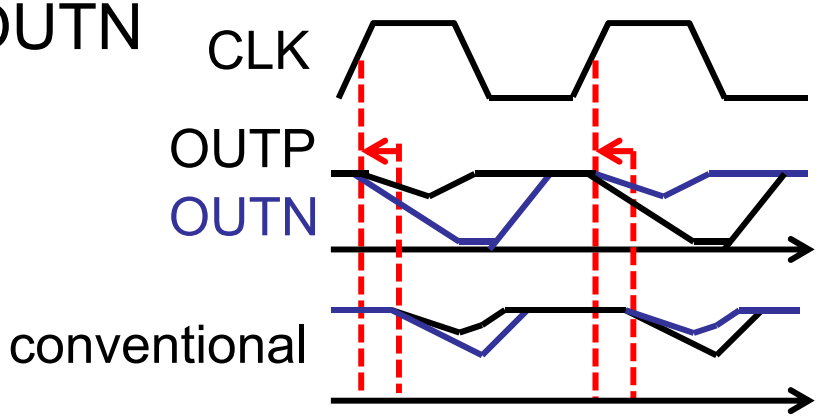
- Tap add block is connected to output
- Current source is driven by a clock buffer



Proposed DFE slicer

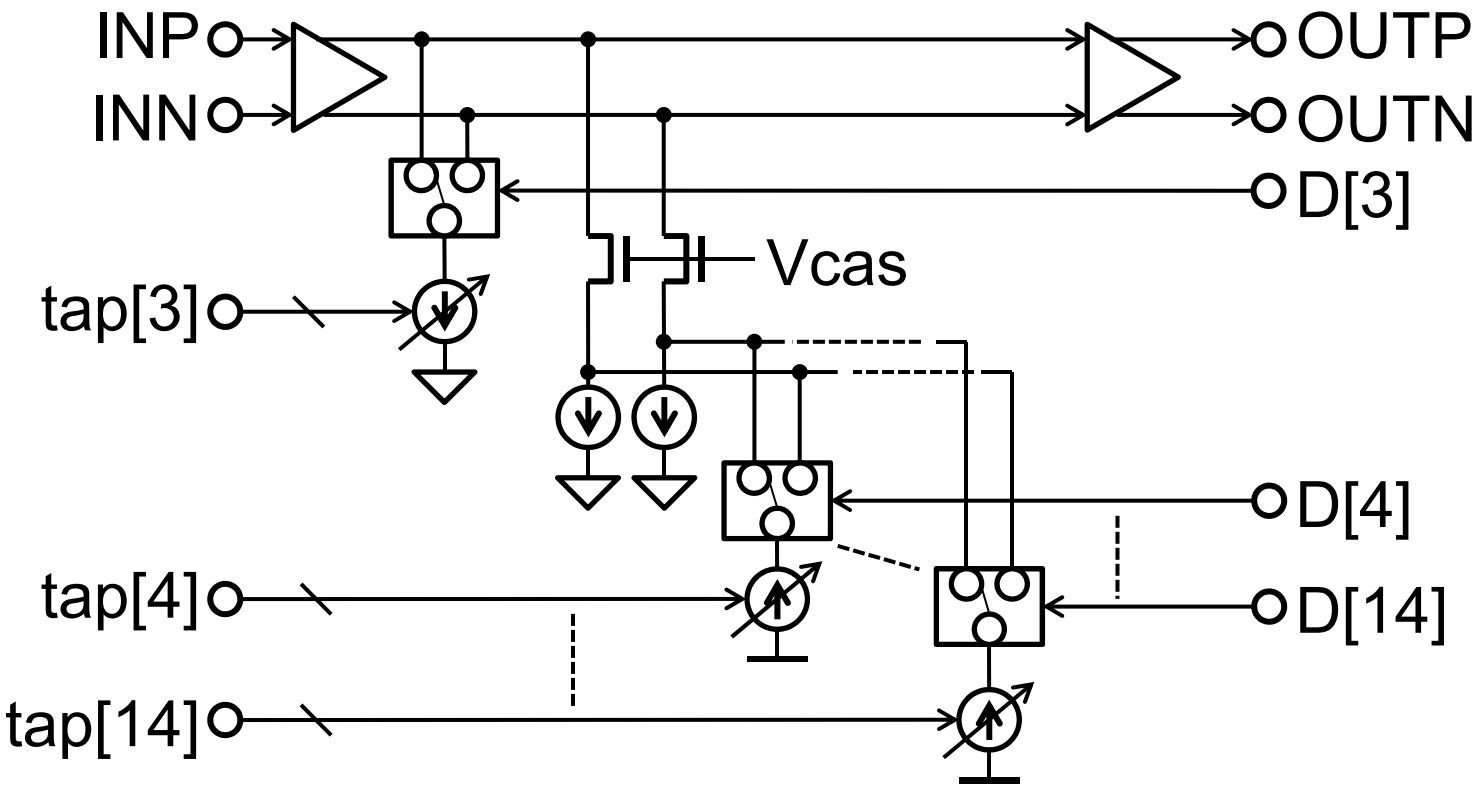
- Tap add block is shared with current source
  ➔ 1.2-mV sensitivity and 60-mV tap range





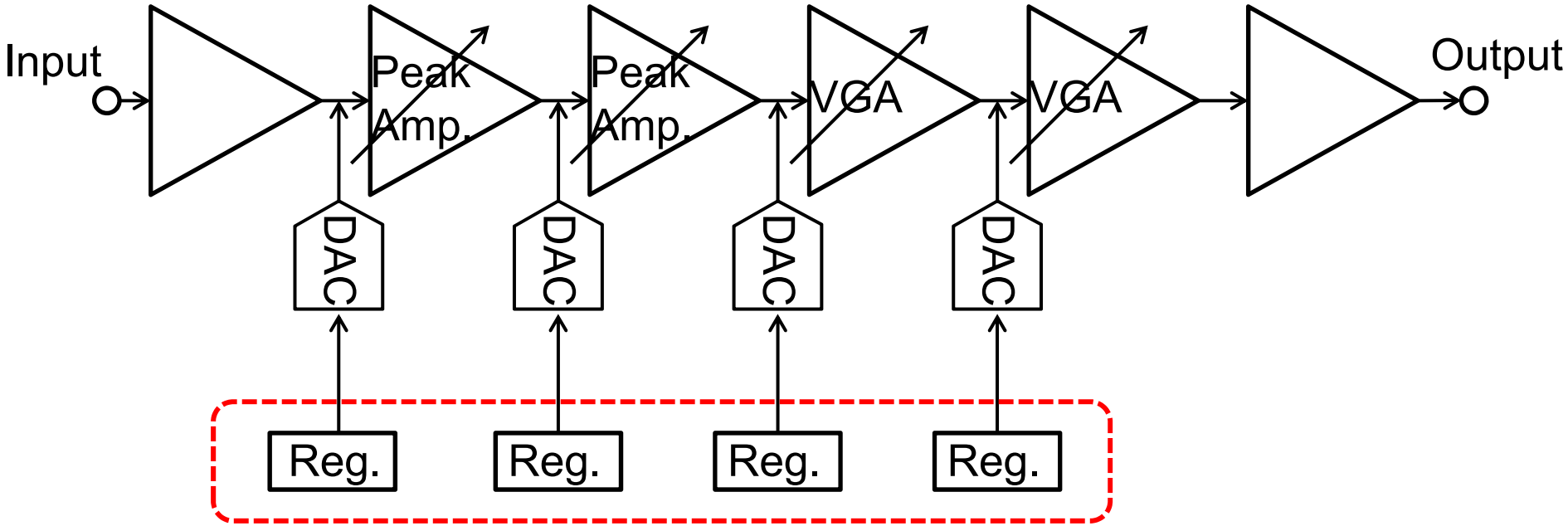
DFE current sum for higher tap

- Adopt a folded cascode to add Tap4 – 14
  ➔ Small parasitic capacitance, small delay



Issue of DC offset cancel

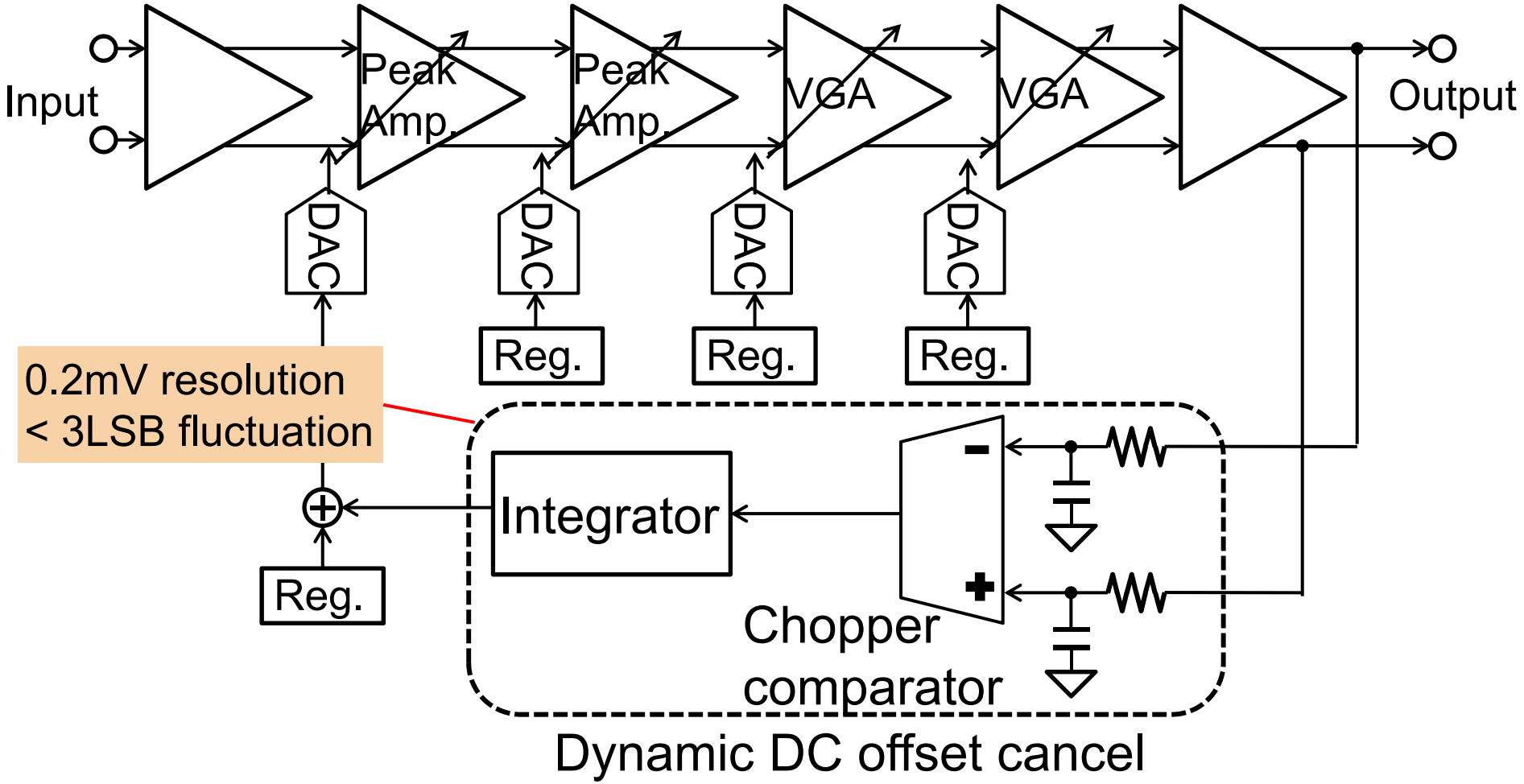
- DC offset target < 1mV
- DC offset shift by environmental variation ~3mV



DC offset compensation values are changed depending on gain setting

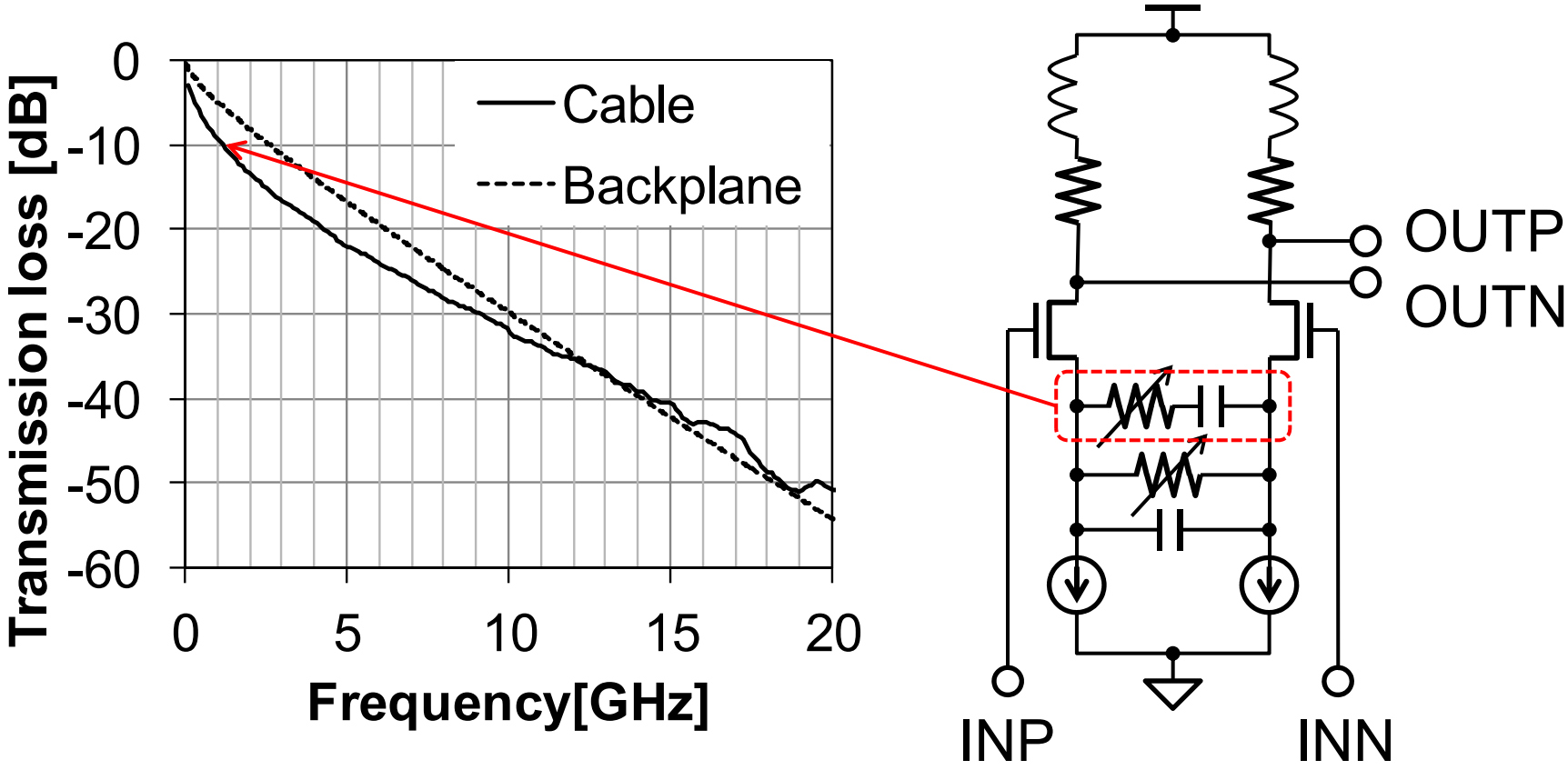
Dynamic DC offset cancel

- Achieve DC offset < 1mV with dynamic DC offset cancel



CTLE with low frequency equalizer

- Adopt low-frequency equalizer for cable

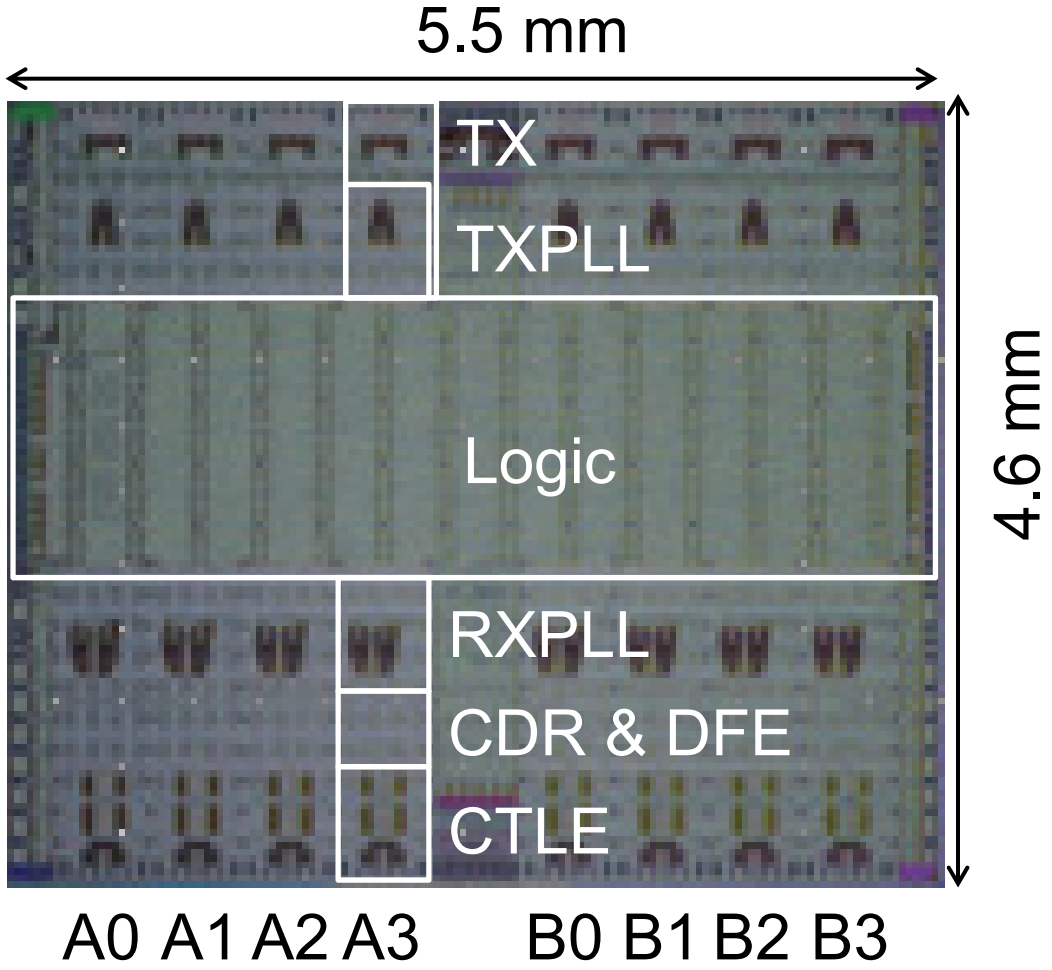


Contents

- Introduction
- Receiver architecture
- Transceiver architecture
  - Proposed slicer in DFE
  - DC offset compensation
  - CTLE with LFE
- Evaluation results
- Conclusion

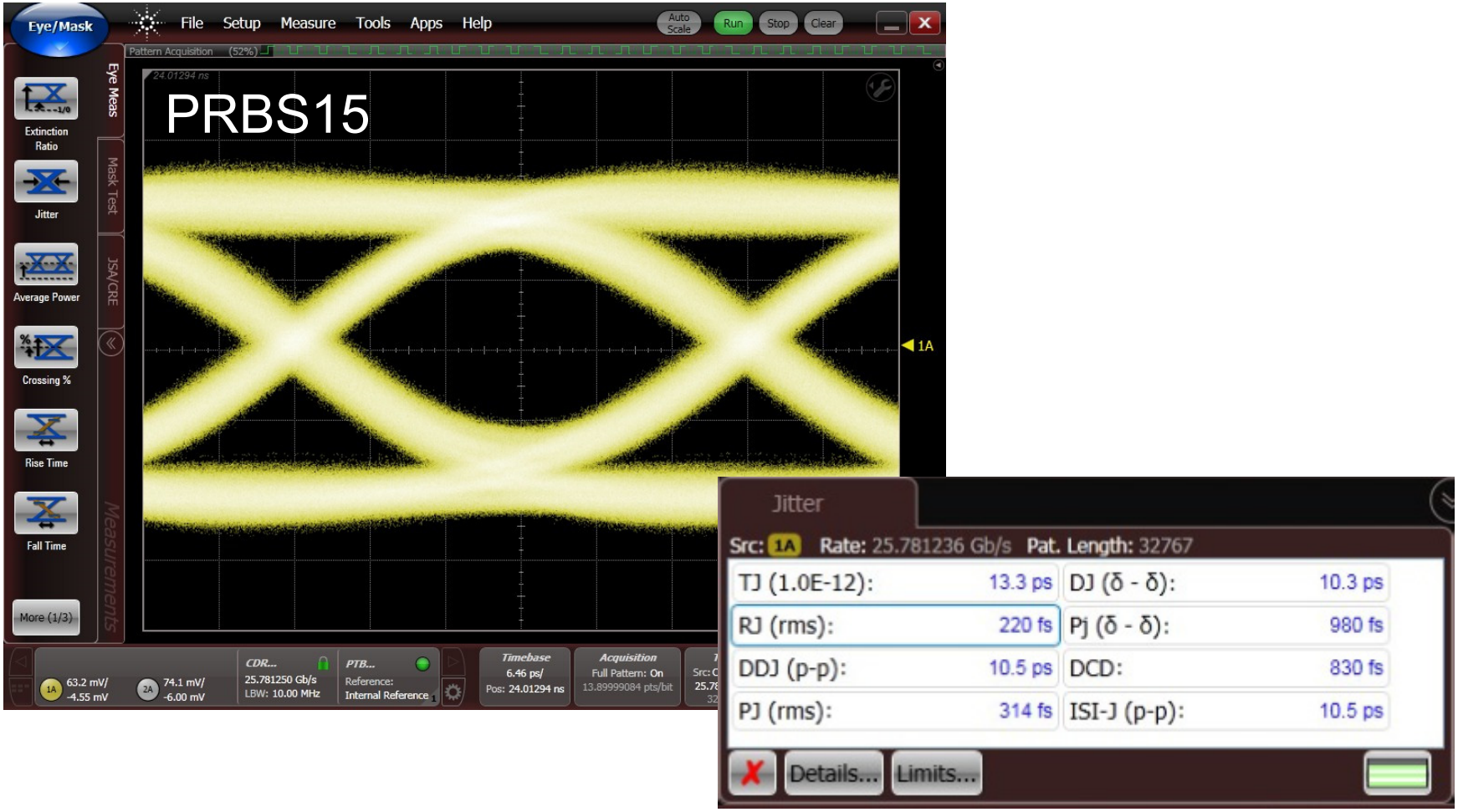
Chip micrograph

8-metal 28-nm CMOS process



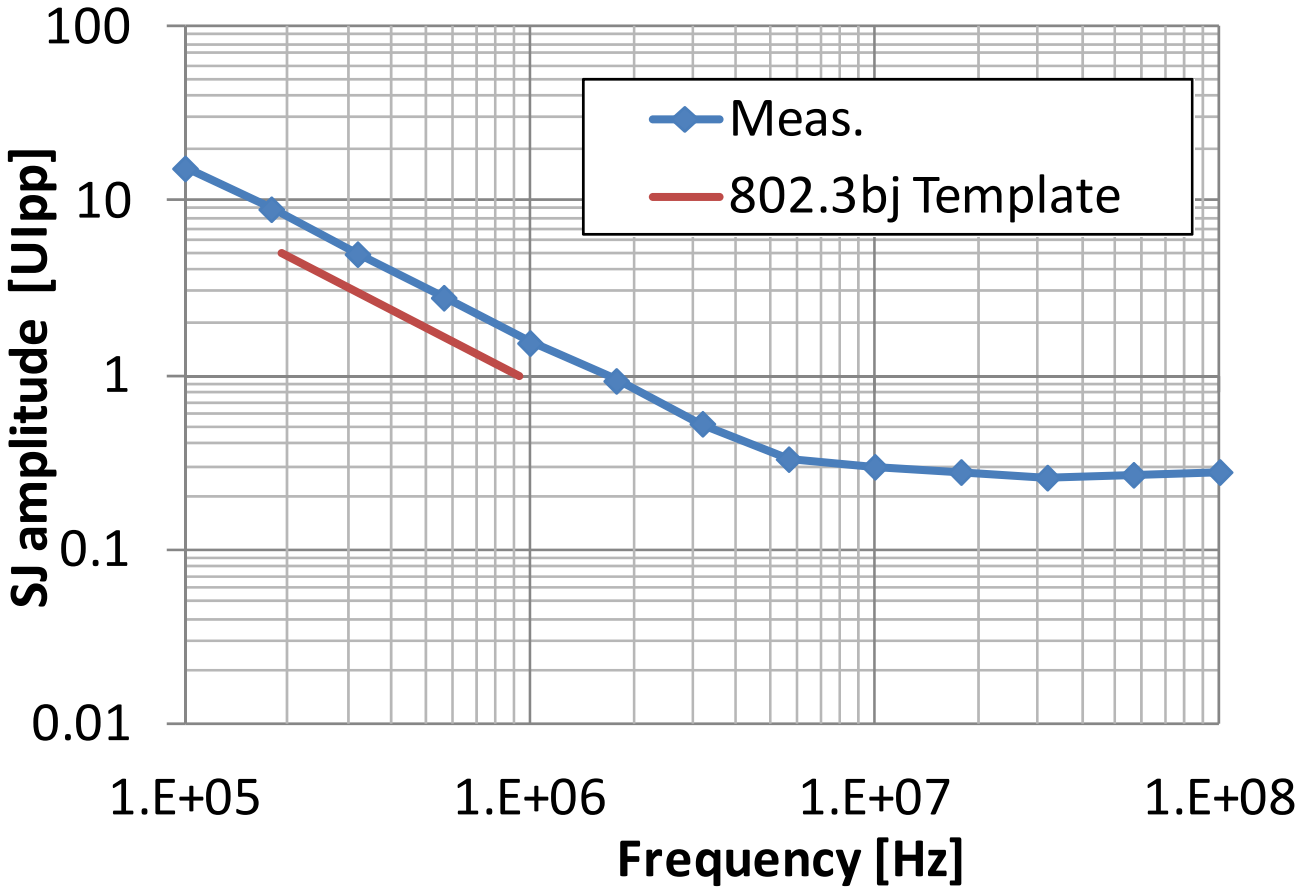
Transmitter output

- RJ at transmitter output is 220fs.

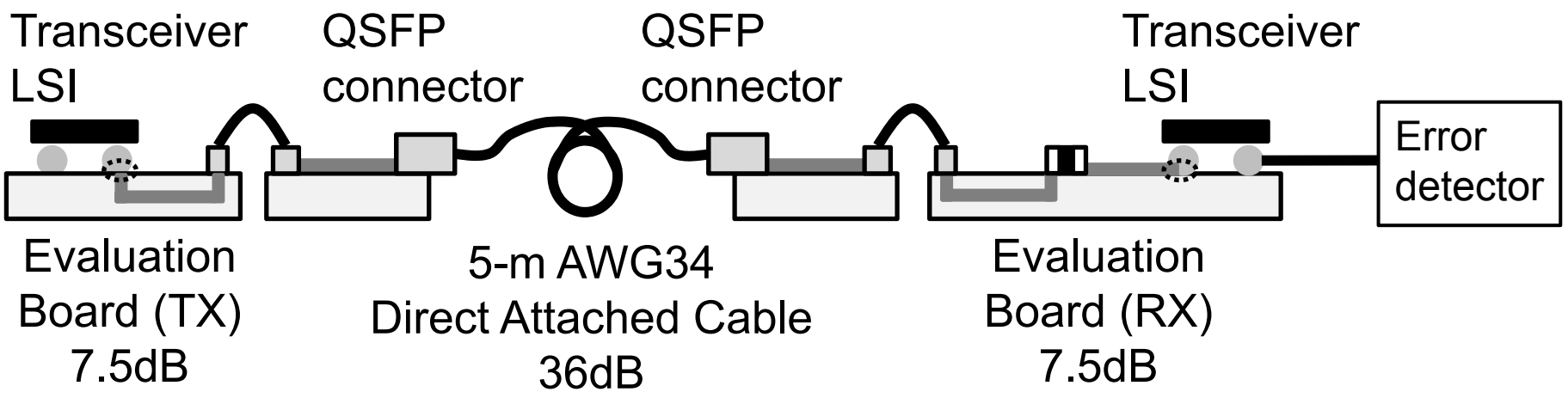


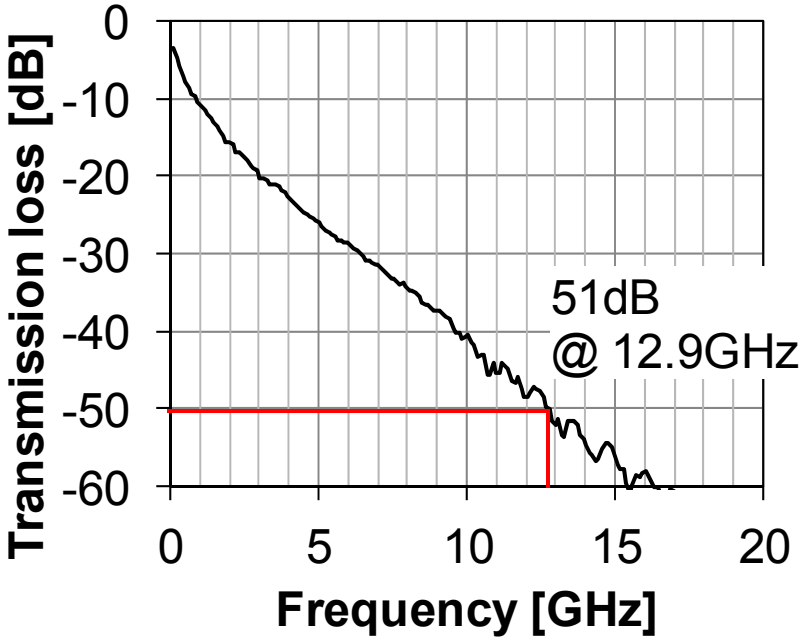
Receiver Jitter Tolerance

•Jitter tolerance is measured with transmitting 25.78-Gb/s PRBS31 data.



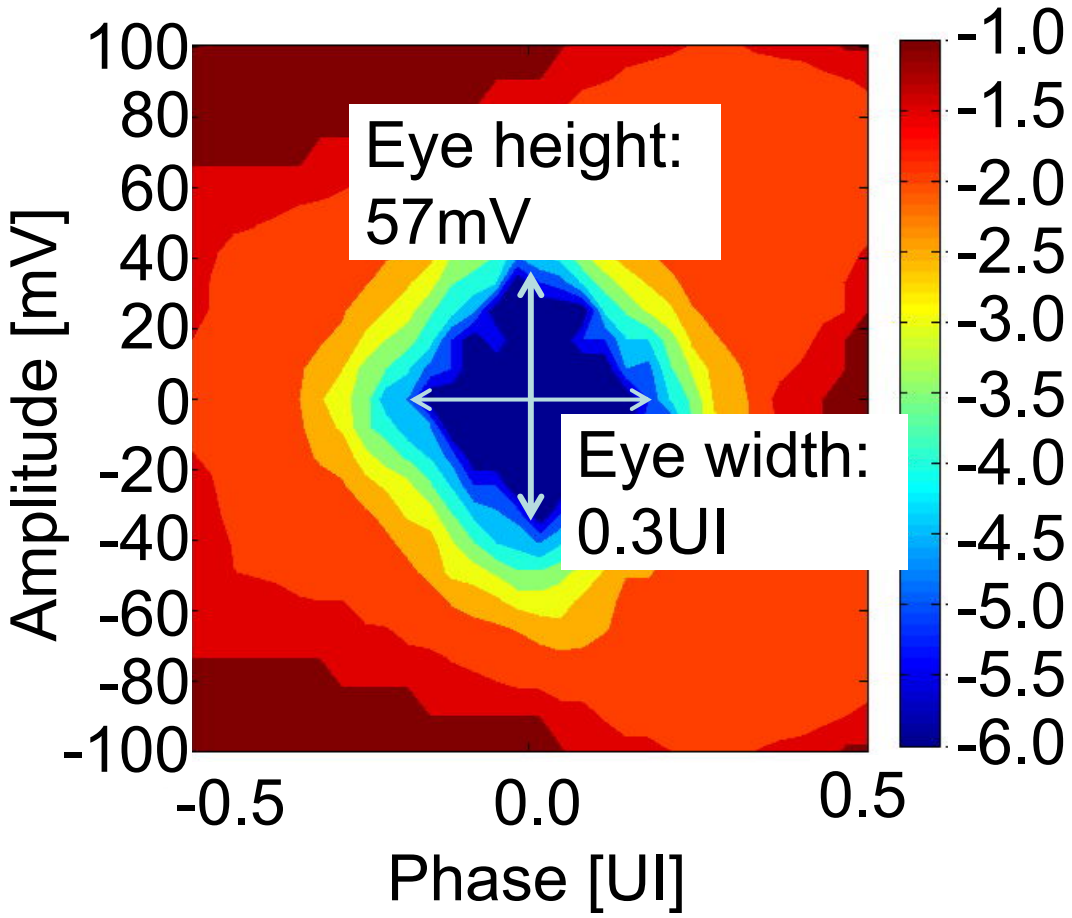
BER measurement setup





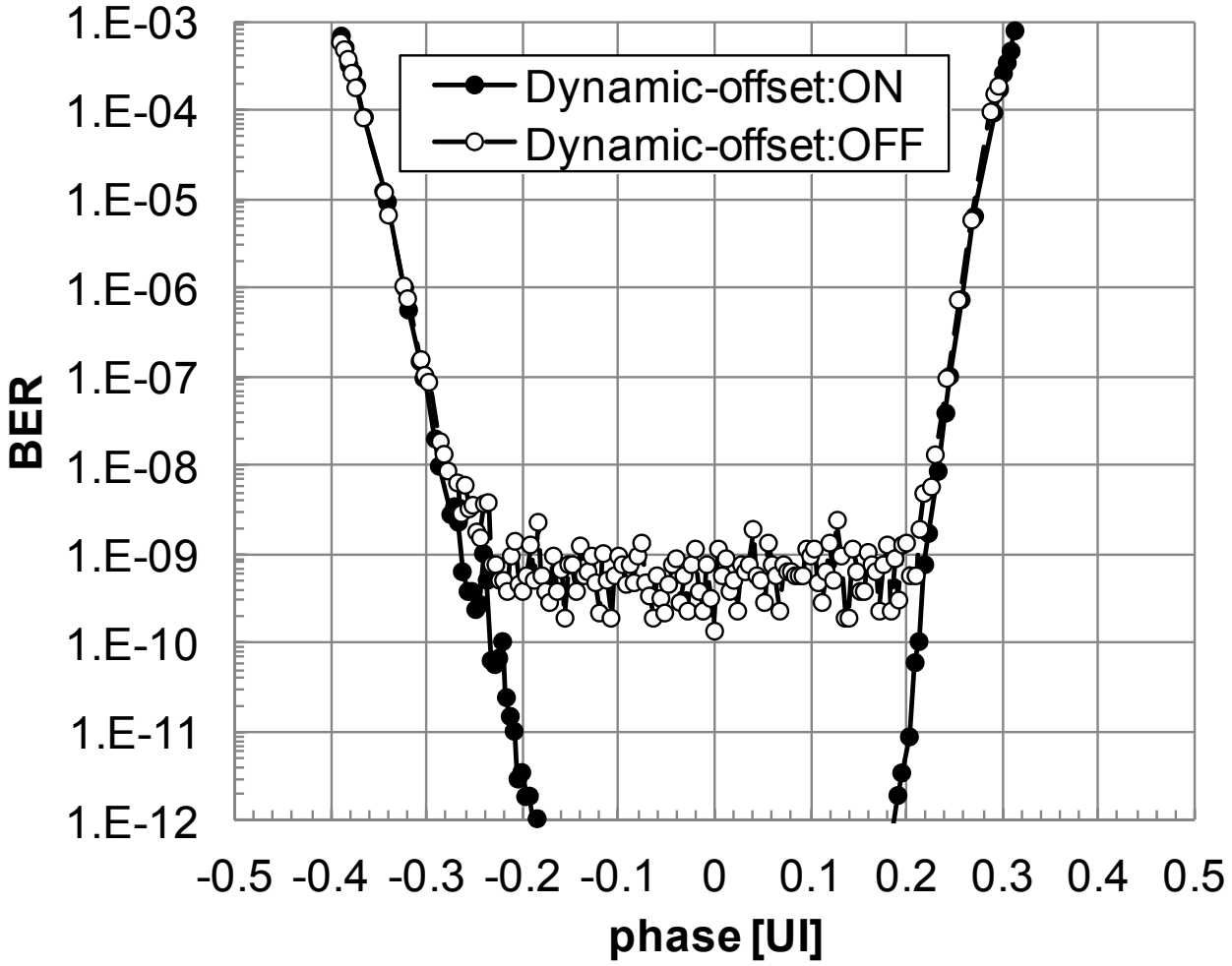
Internal eye monitor output

- Enough eye opening with CTLE w/ LFE and DFE w/ proposed slicer



BER measurements

- BER w/ dynamic DC offset cancel < 10^{-12}



Performance comparison

	Bulzacchelli ISSCC 2012	Kimura ISSCC 2014	Kawamoto ISSCC 2015	Zhang ISSCC 2015	This work
Technology	32-nm SOI CMOS	28-nm CMOS	28-nm CMOS	28-nm CMOS	28-nm CMOS
Transmission loss [dB]	35	34	40	40	**51**
Power consumption [mW/lane]	693	560**	648	295**	403 346**
Data rate [Gbps]	28.0	28.0	25.8	25.8	25.8
FoM* [pJ/bit/dB]	0.707	0.571**	0.628	0.286**	0.313 **0.269****

$$* \; FoM\,(pJ/bit/dB) = \frac{Power\ consumption}{Data\ rate \cdot Channel\ loss}$$

***Analog only*

Contents

- Introduction
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Conclusion

- A 25-Gb/s serial-link transceiver equalizing 50-dB loss copper cable is presented.
- Two key technologies enables to equalize 50-dB loss channel with low power consumption.
  - A bias controlled tap slicer has high sensitivity in operating at 25Gb/s with wide tap range.
  - A sub-mV dynamic DC offset cancel improves SNR at the receiver input.
- The transceiver can transmit data through 51-dB loss channel with BER < 10^{-12}.
- It consumes 403mW on 0.9 and 1.5 V supplies.

Acknowledgement

- K. Nakajima, N. Sezaki, M. Ogihara, J. Tanaka, T. Funada, K. Kawamura, F. Nagasaki and S. Suzuki for system architecture discussion
- T. Hiyama, K. Miyamoto, M. Nakayama, S. Ueno, T. Ido, M. Kokubo, and K. Watanabe for project support

A 40/50/100 Gb/s PAM-4 Ethernet Transceiver in 28nm CMOS

K Gopalakrishnan[1], A Farhood[1], A Ren[1], A Tan[1],
A Tiruvur[1], B Helal[1], C Loi[2], C Jiang[1], H Cirit[1], I Quek[2],
J Riani[1], J Gorecki[1], J Pernillo[1], J Wu[1], L Tse[1], M Le[3],
M Ranjbar[1], P Khandelwal[1], R Narayanan[1], P Wong[1],
R Mohanavelu[1], S Bhoja[1], S Herlekar[1], V Shvydun[1]

[1] Inphi, Santa Clara, CA,
[2] Inphi, Singapore, Singapore,
[3] Inphi, Irvine, CA

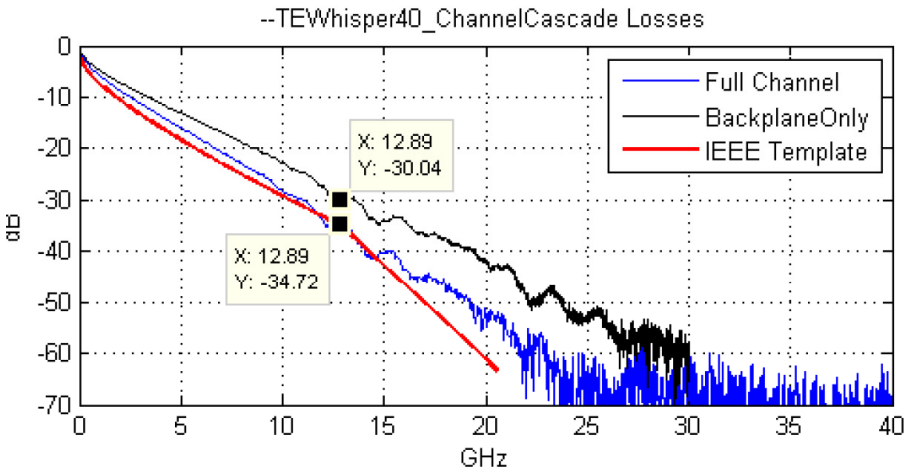
Outline

- Motivation and Objectives
- Transceiver Features
- Transmitter Path
- Receiver Path
- PLL
- Regulator
- Performance summary
- Conclusion

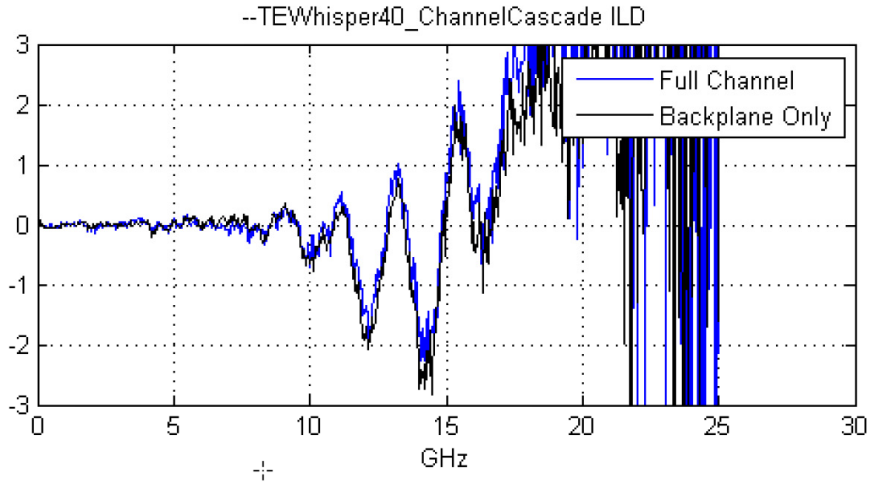
Motivation

- Cloud infrastructure is driving everything!
  - Demanding higher performance and aggressive cost
  - Optical Modules are critical part of this infrastructure
- Addressing cost of optical modules by reducing the number of optical components
  - Current generation of 100G modules use 25Gbps per λ
  - more bits/wavelength = increasing modulation
- Backplanes at 25GHz pose significant challenges
  - High Insertion loss deviation (ILD) and Insertion to crosstalk ratio (ICR)
  - PAM4 enables legacy systems for 56Gbps / link

Motivation



Insertion Loss (IL)

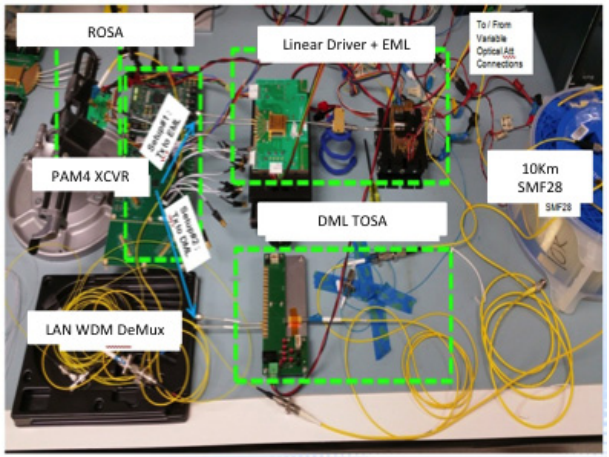


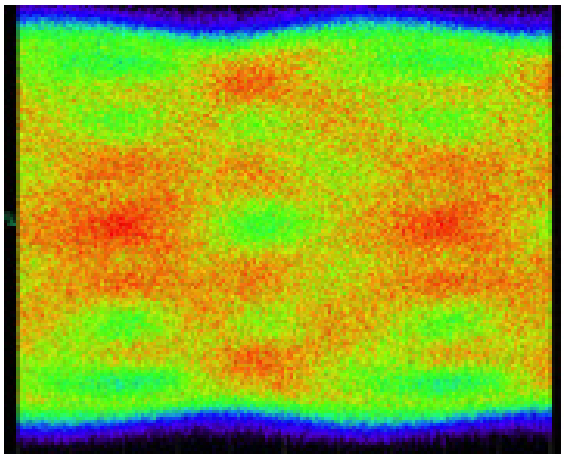
Insertion Loss Deviation (ILD)

- Significant insertion loss and ILD
- PAM-4 more sensitive to ISI
  - Group delay variations
  - Eye can be closed with very little channel loss
- Precise cancellation of ISI is key

Motivation

- Optical systems are not loss limited
  - Wide range of non-idealities (signal dependent noise, signal dependent BW and reflections)



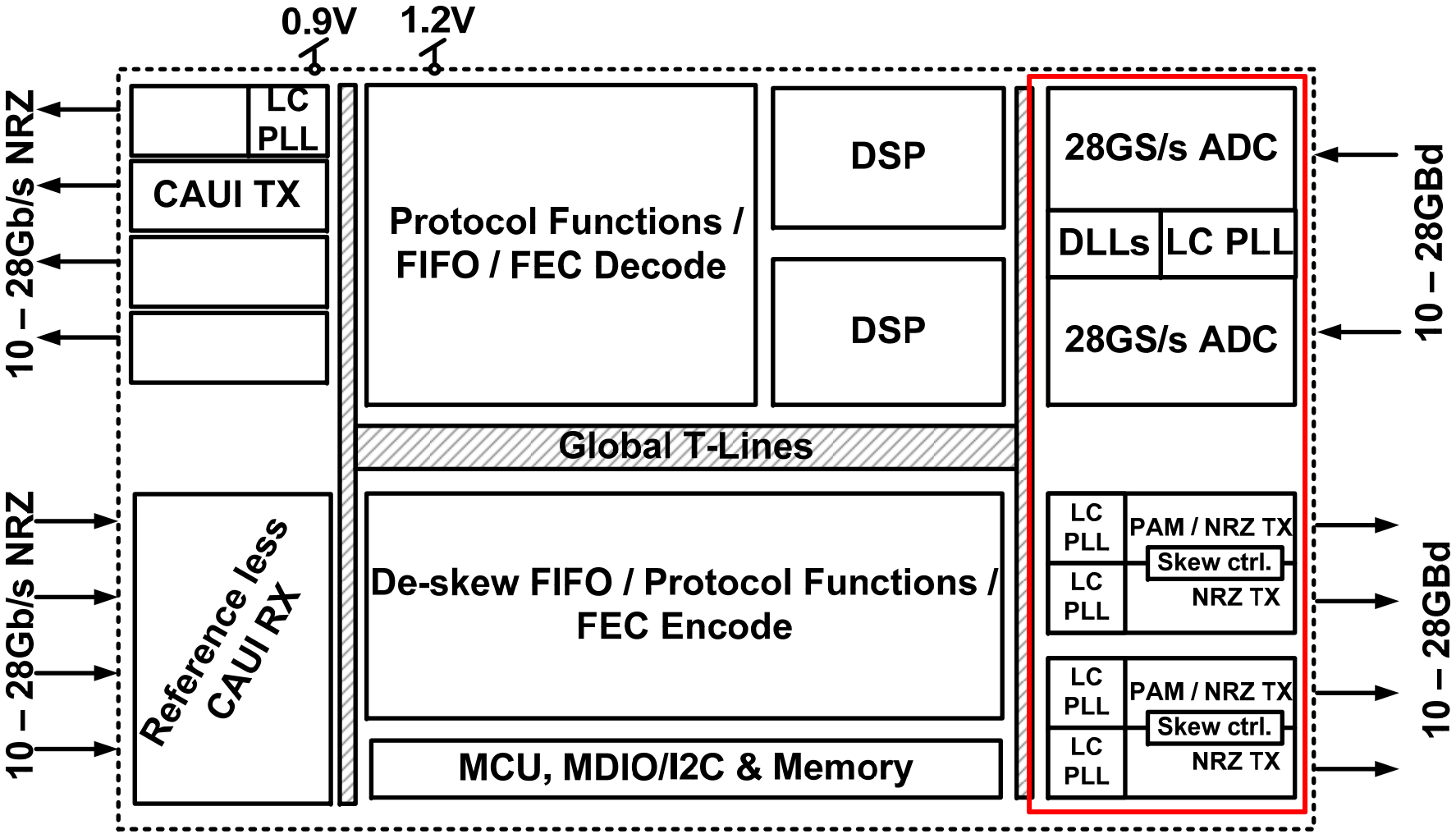


- ADC-DSP
  - Flexibility to deal with wide range of channel impairment and provide robustness
  - Allows soft decisions to be used in error correction schemes

Multi-rate PAM-4 Transceiver

- Support 100G dual-λ and 40G single-λ systems
- Support segmented optics that generate PAM4 optically
- Close legacy backplane links at 50Gbps/link with sufficient link margin
- NRZ ↔ PAM4 to enable systems in transition to PAM-4
- Multiple High-gain FEC for optical/electrical applications
- 1.2V Analog and 0.9V Digital supply

Chip Block diagram

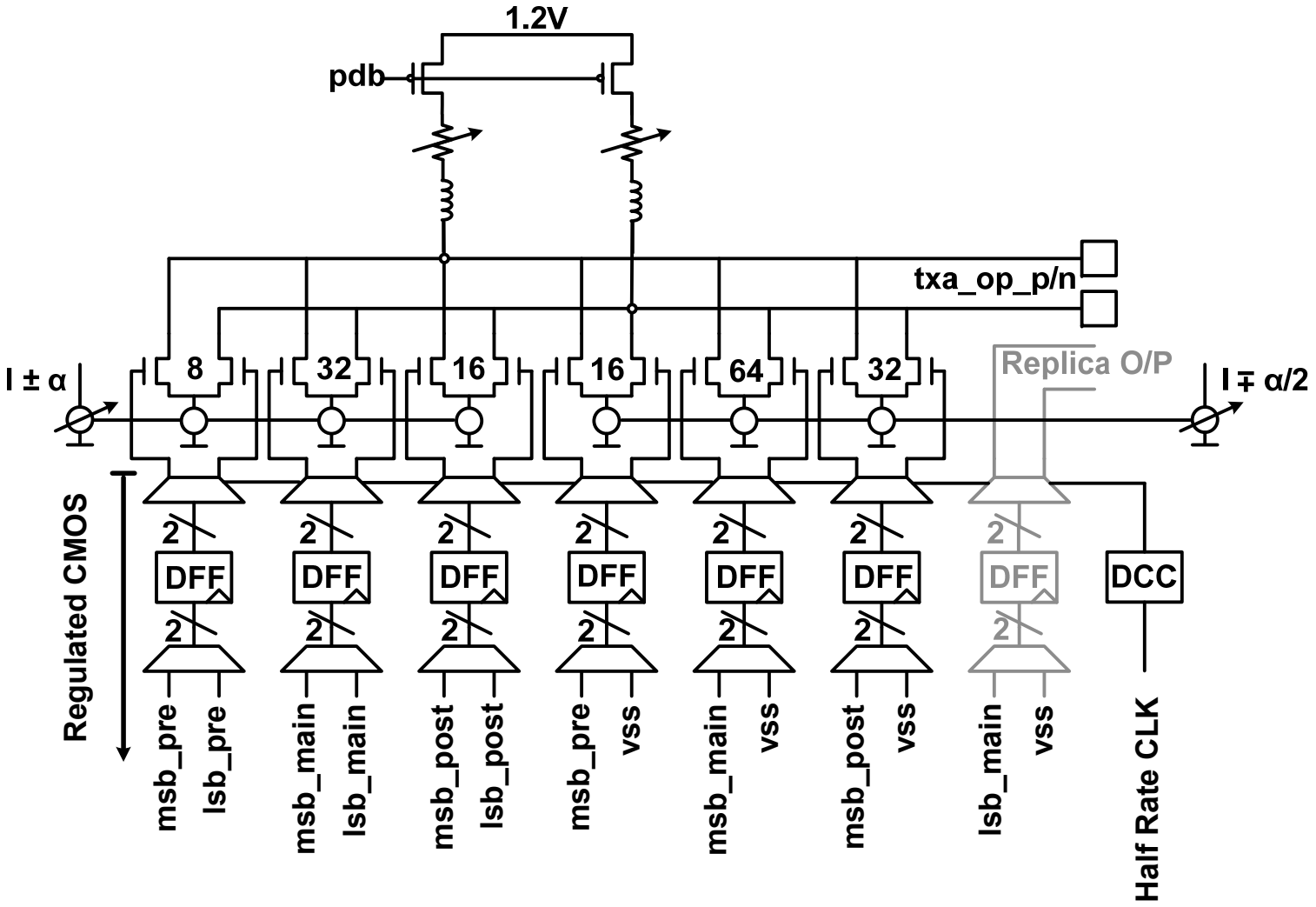


This presentation

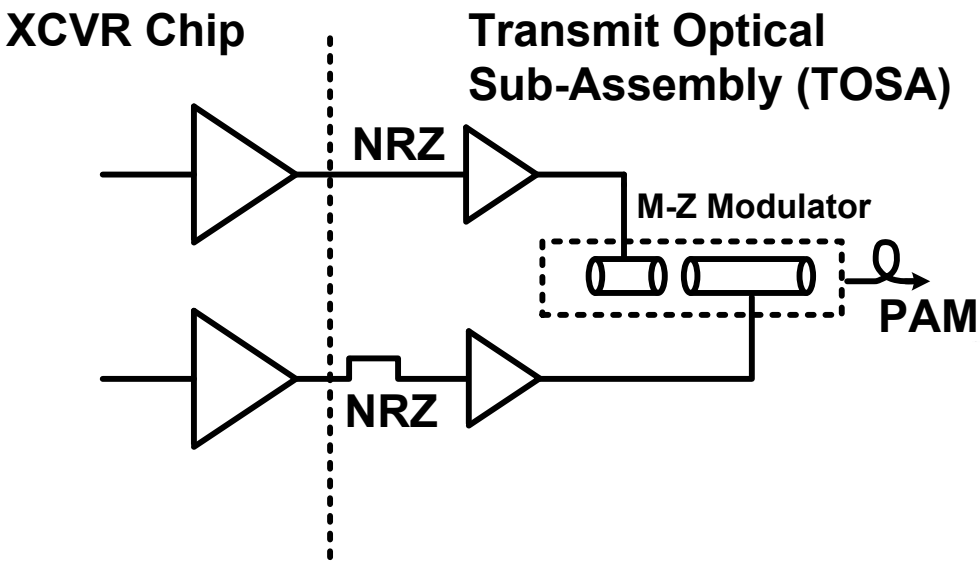
Key Architectural Approaches

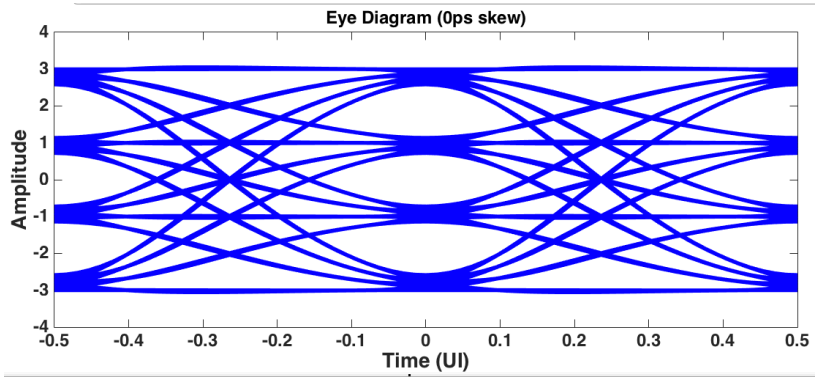
- CML Driver with CMOS backend
  - Enables wide swing range and low power
- ½ rate TX Clocking and ¼ Rate RX Sampling
- 7-bit ADC-DSP based receiver with SAR core
- The clock path is CMOS based with regulators providing the required power rejection
- The data path are under independent regulator domains for proper isolation
- Multi-Tap FFE / DFE and Calibration in the DSP

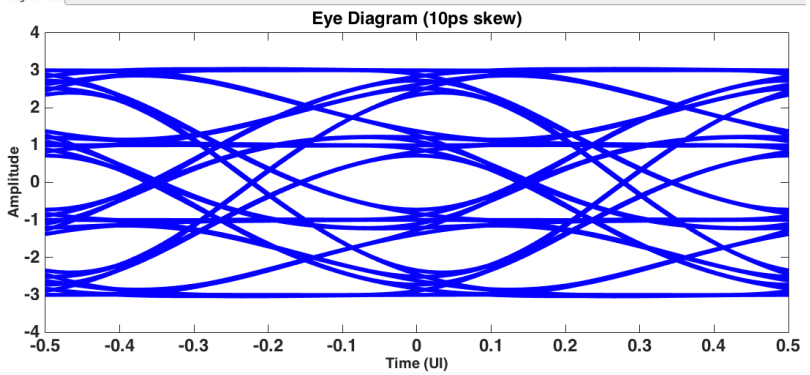
PAM-4 Transmitter



Segmented driver



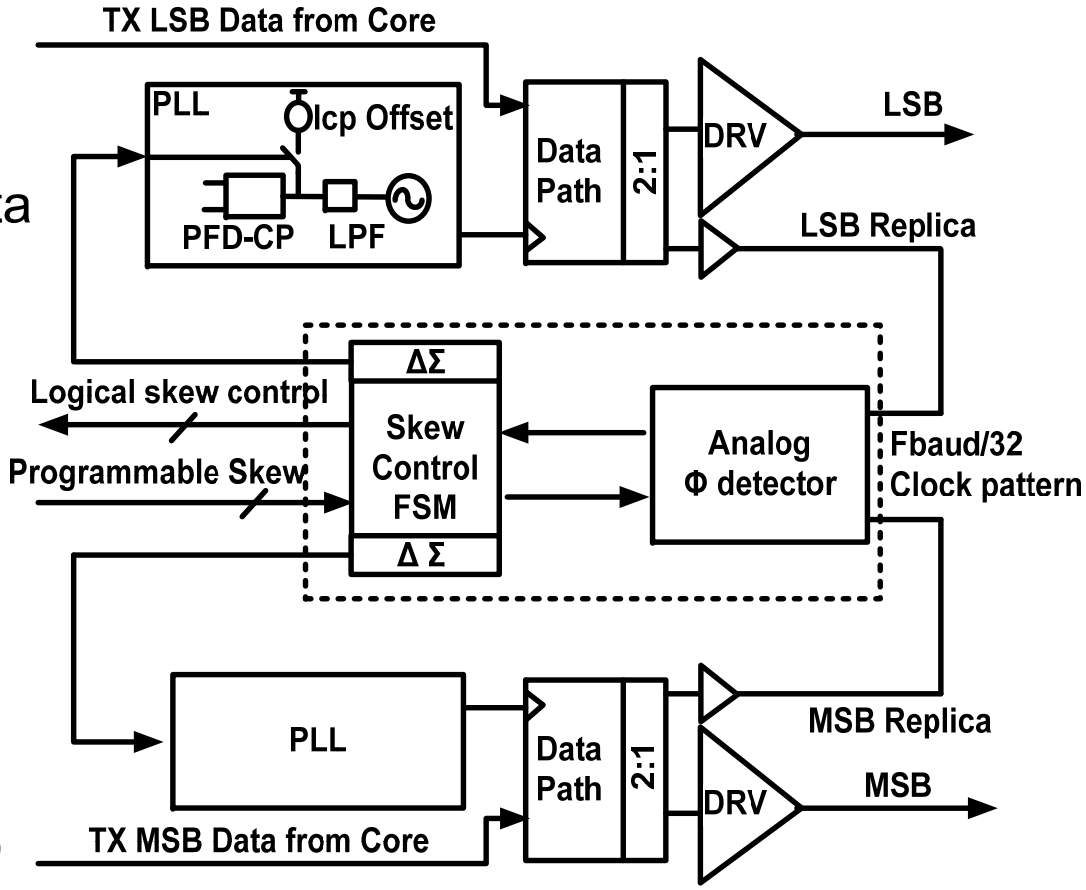




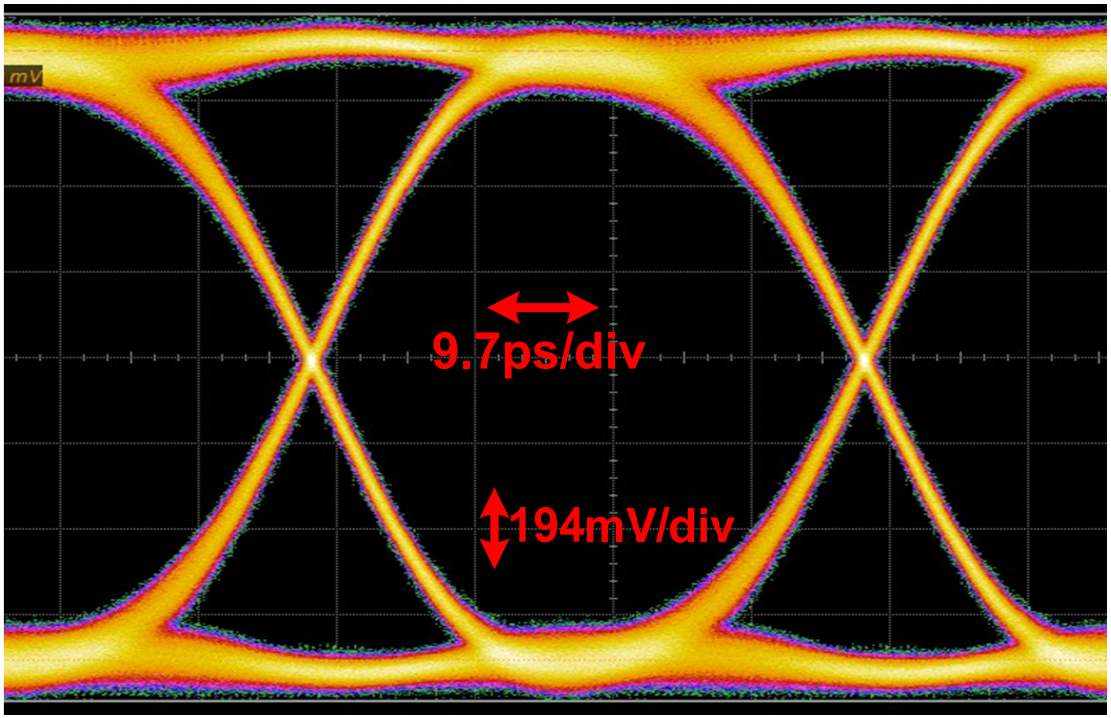
- PAM-4 signal generated optically using segmented Mach-Zehnder
- Skew in this scenario can be very large relative to the UI

Segmented driver

- Drivers output NRZ
- Replica path generates F/32 clock
- Logical skew adjusted via data path bit pointers
- Sub-UI skew is corrected by adjusting charge pump offset in the PLLs
- A 2nd crder ΔΣ used to increase the resolution
- FSM periodically auto-zeroes analog ϕ-detector
- Gain calculated from 0UI (no delay) and 1UI (known delay)

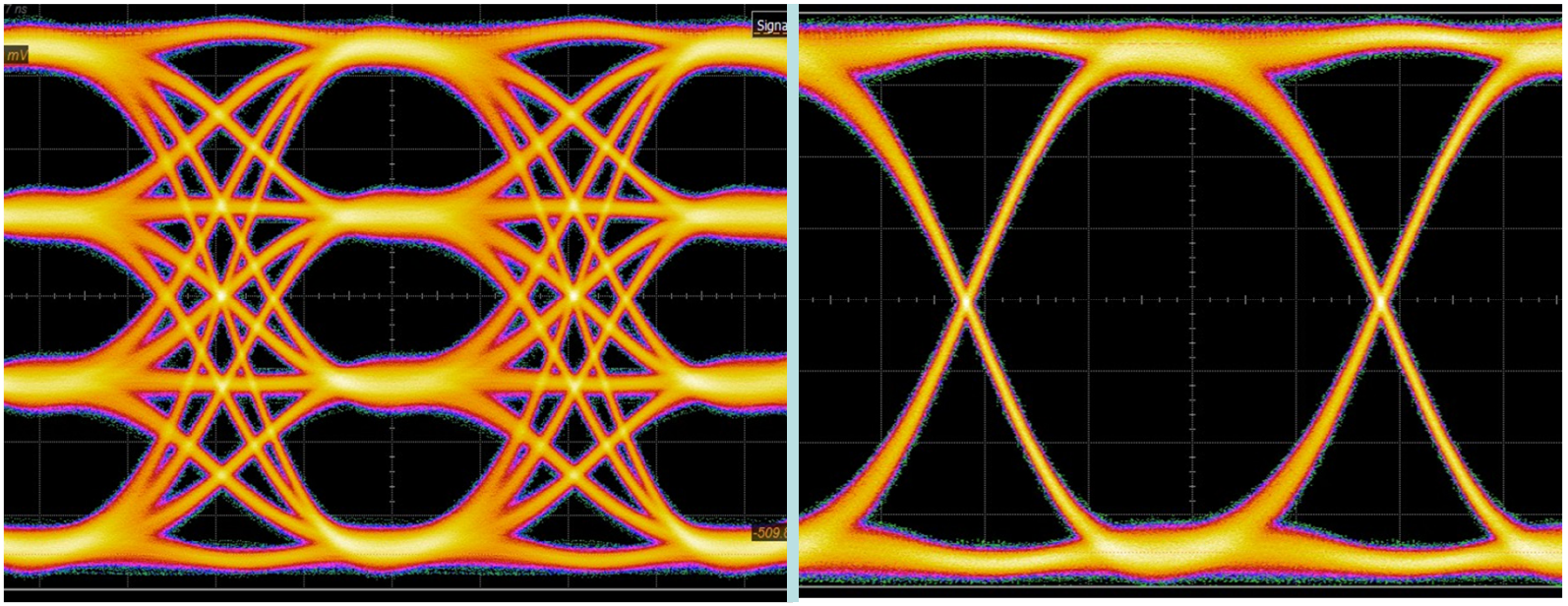


NRZ TX Measurement



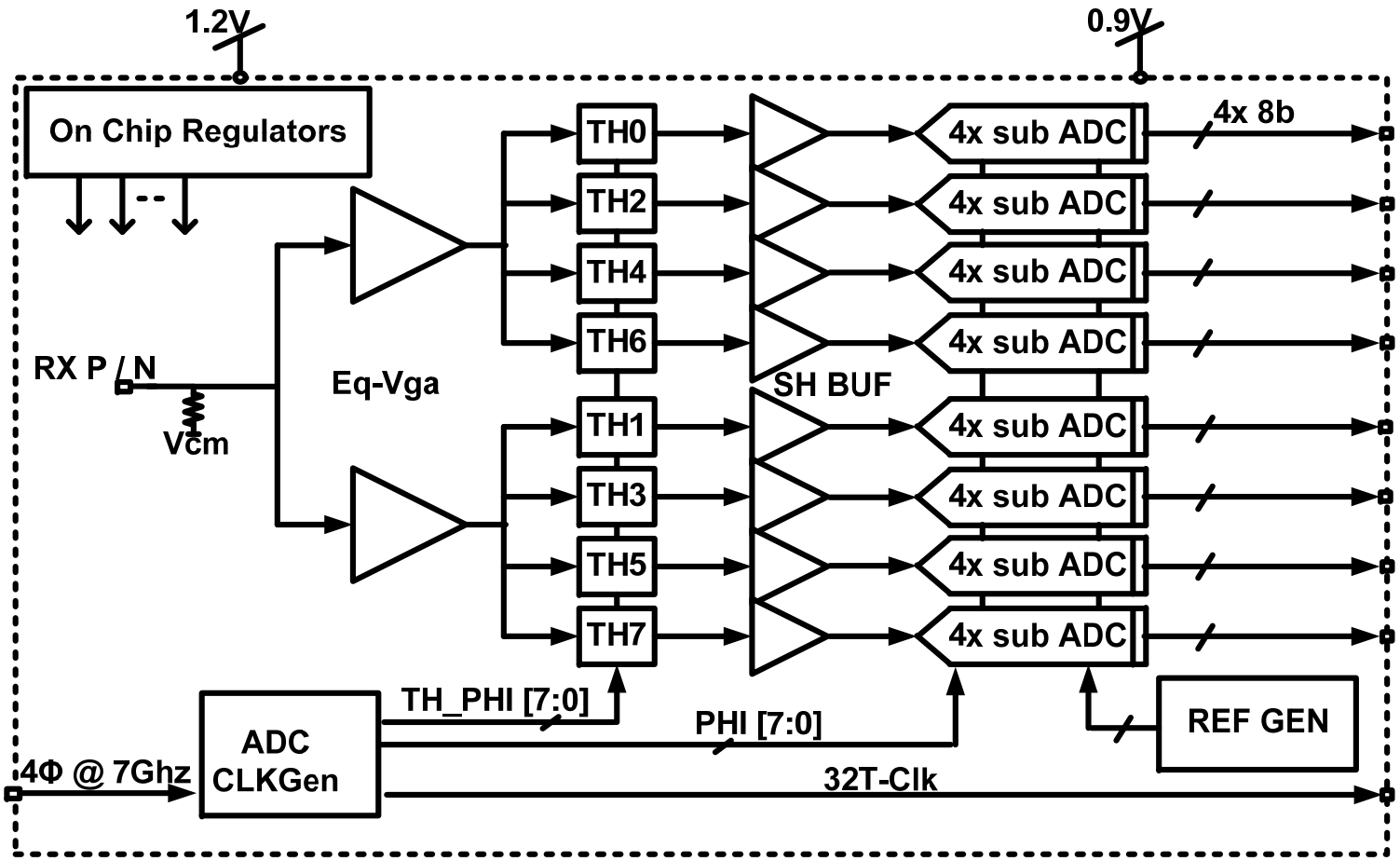
- Electrical outputs of XCVR chip
- 25GBd NRZ with a PRBS15 pattern
- Golden CDR: 2MHz 1st order

PAM-4 TX Measurements



- Electrical outputs of XCVR chip
- PAM-4 with same output swing and rate (25Gbd)
- SNDR measurements show better than 33dB

PAM-4 Receiver

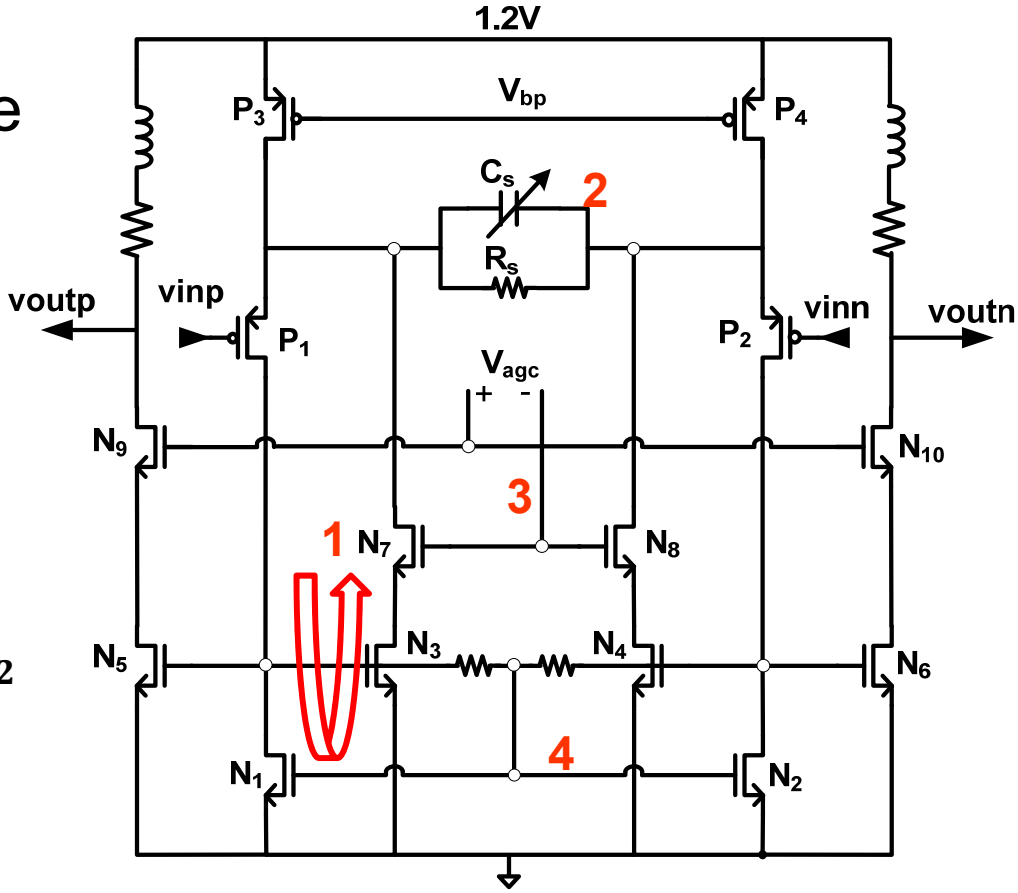


EQ / VGA

1. Gm-boosted source degeneration to improve distortion
2. EQ control
3. Gain control for ADC
4. Self biasing for the loop

$$HD_2 \propto \frac{\omega}{\omega_s}\frac{vid}{vov_p}$$

$$HD_3 \propto \frac{1}{(1+Gm_p.R)}\frac{\omega}{\omega_s}\left(\frac{vid}{vov_p}\right)^2$$

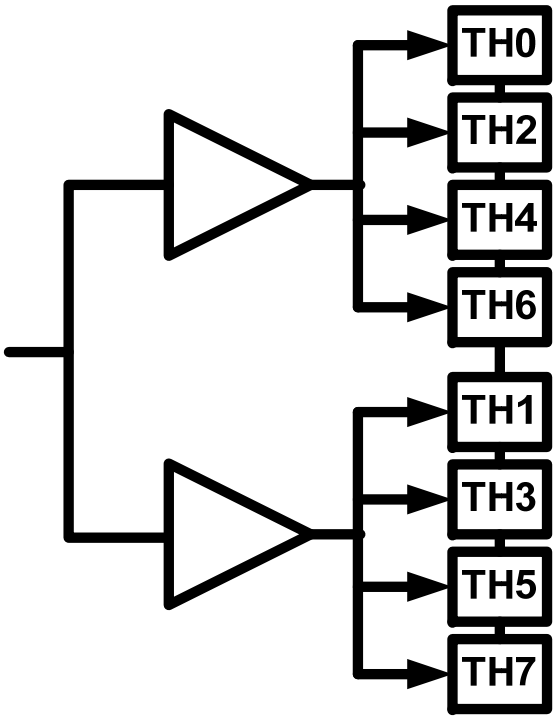


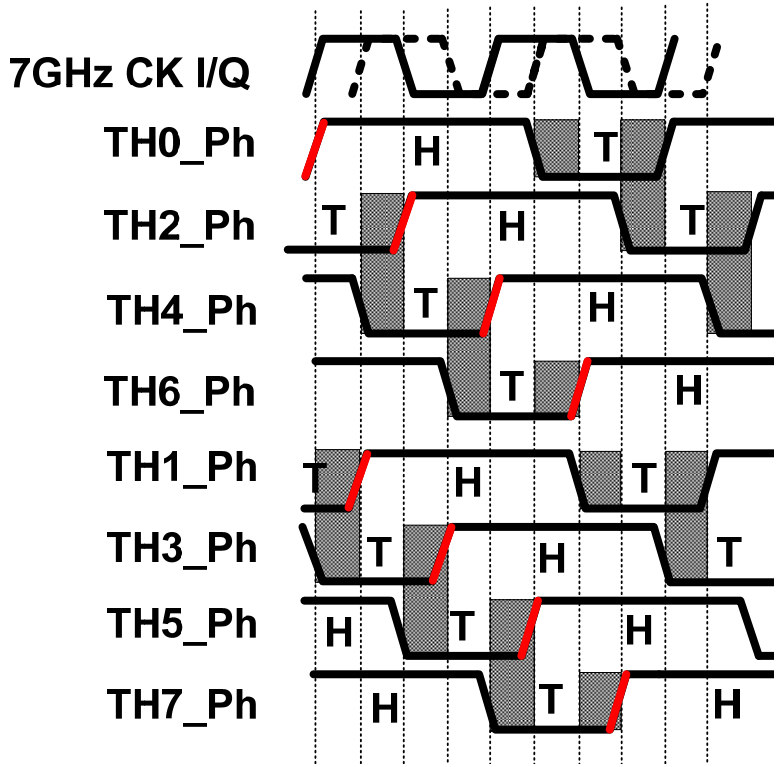
Vid = Input differential voltage

Vov = overdrive voltage of PMOS input pair

Gm_p = boosted gm of input diff pair

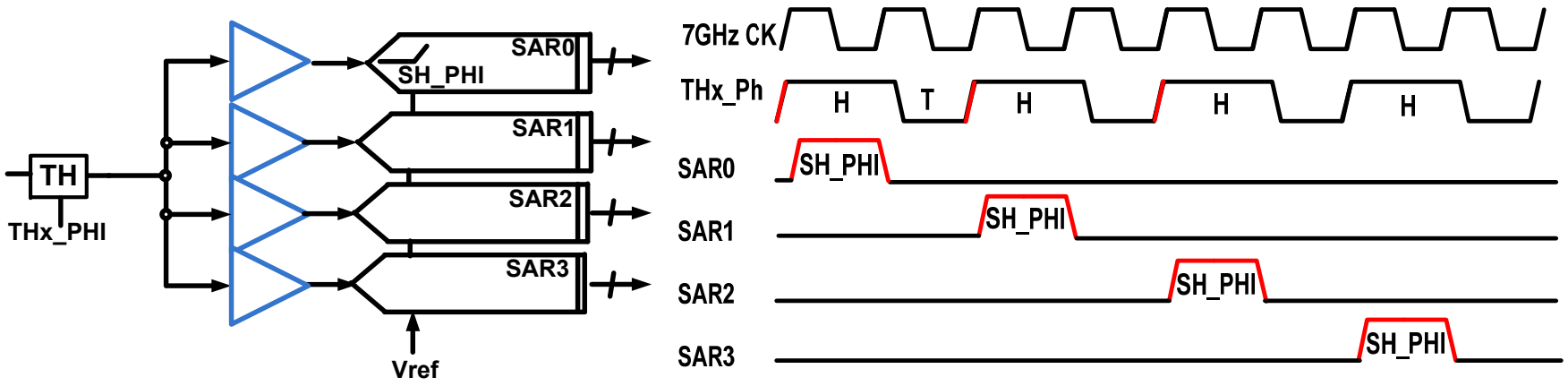
VGA – T/H





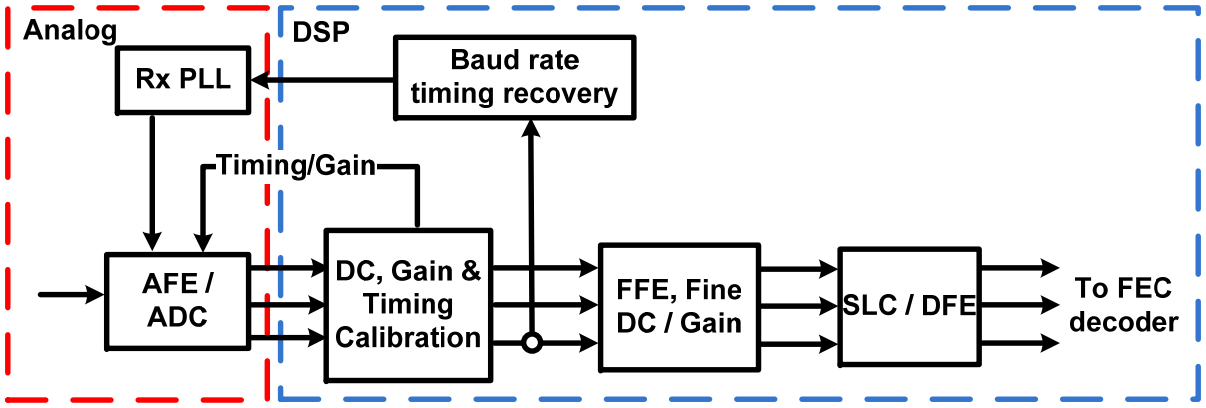
- Even/Odd T/H channels separated for relaxed settling
  - reduced Even-odd interaction
- No more than 2 T/H's load the VGA at any given time illustrated by the gray zones

7b SAR Core



- T/H to S/H hand-off shown in timing diagram above
- Coarse gain trimming for every T/H Channel
- The SAR core achieves a simulated SNDR > 41dB over all process, voltage, temperature and frequencies
- Metastability rate of the SAR data path < 1e-13

DSP Architecture

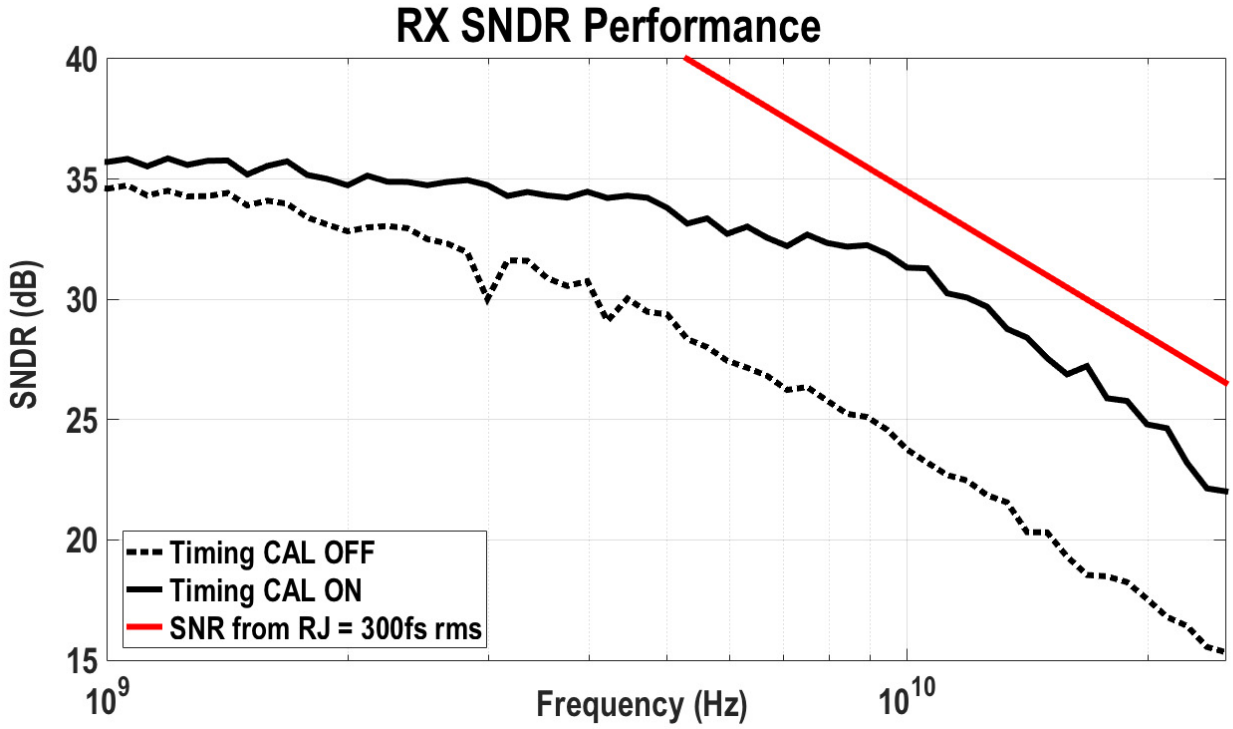


- Gain, offset and timing calibration loops closed through the DSP
- Baud-rate sampling architecture:
  - M&M Baud-rate timing recovery
  - T-spaced FFE and non-uniform sampler or 1-tap DFE
  - Fully adaptive receiver

AFE Calibration

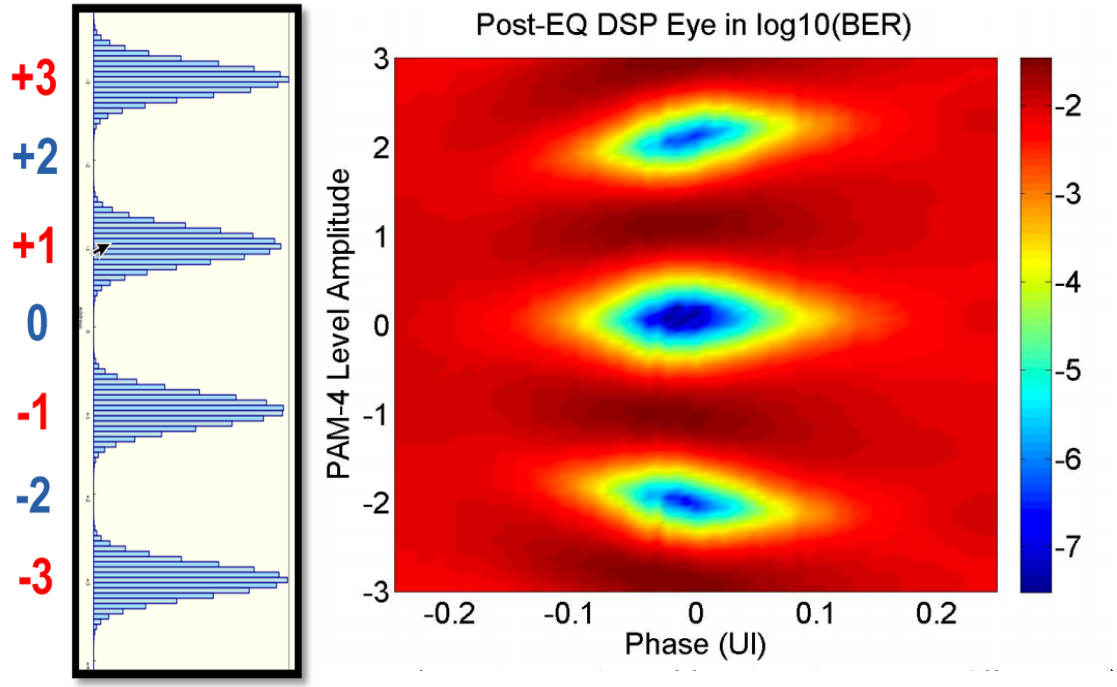
- Independent offset calibration loops for each one of the 32 interleaved AFE channels
- Coarse gain mismatch is corrected in analog
  - based on simple envelope detection scheme in the DSP
- Fine gain calibration is fully digital
- Timing calibration using correlated properties of the PAM signal
  - Trims delay cells on each T/H sampling phase

Receiver Measurements



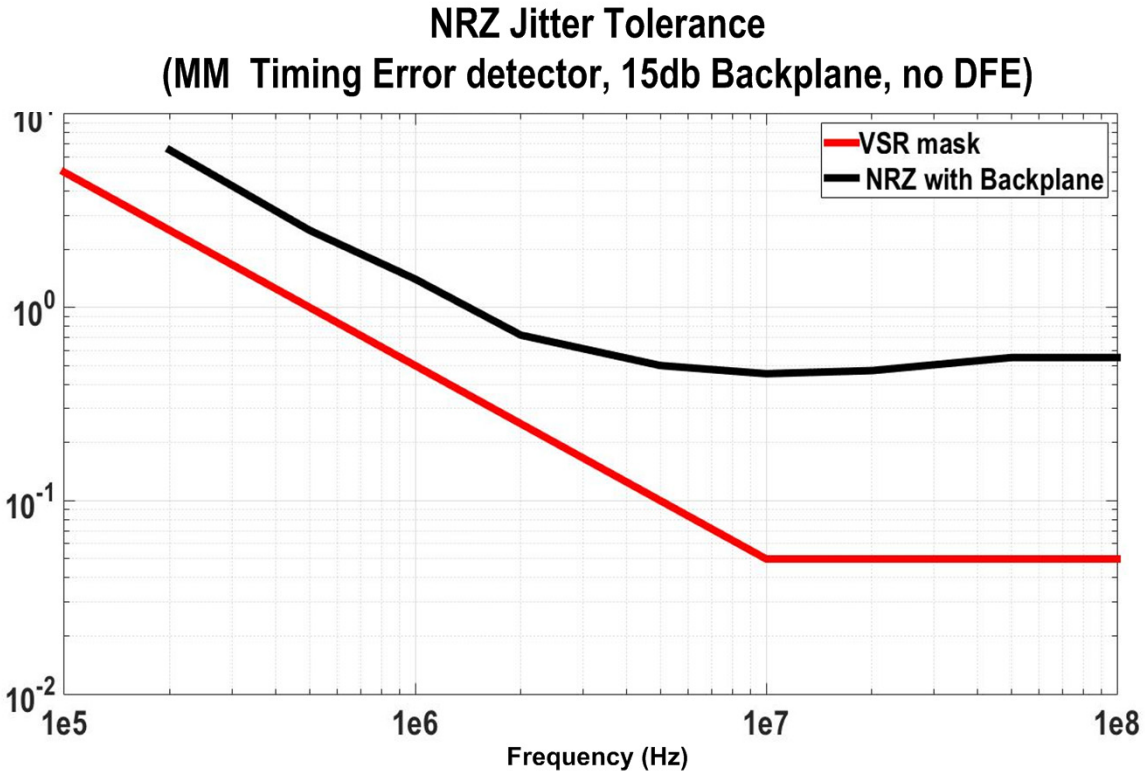
- Measured with 90% full scale and Fs = 25GS/s
- Measurements were done with CDR frozen. In-band RJ is pessimistic in this measurement.
- Estimated jitter in sampling clock (including PLL) is ~300fs rms

Receiver Measurements



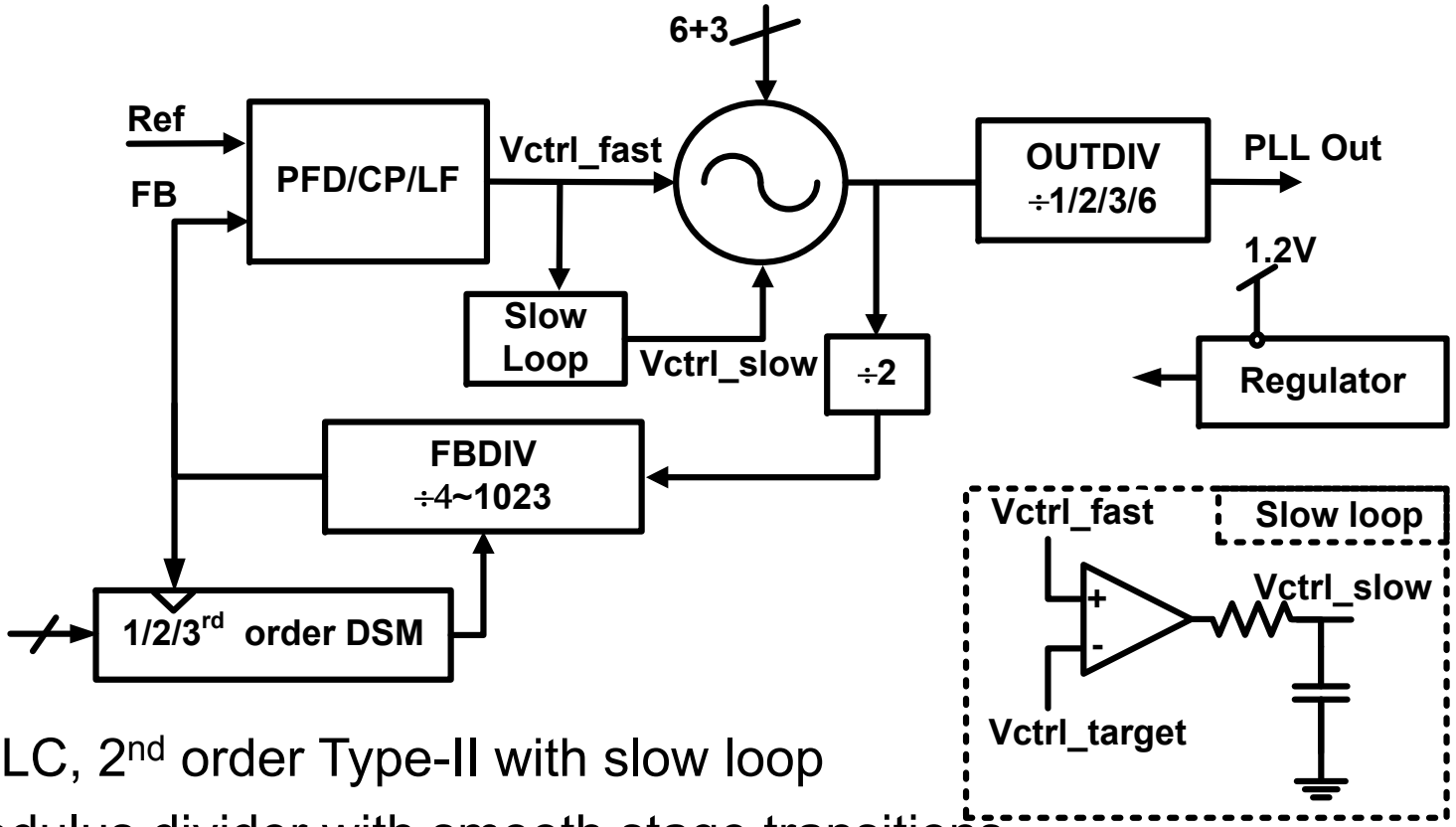
- 40” Backplane with ~35dB loss at 12.5GHz
- 2mV rms of ICN (Integrated cross-talk noise) was added
- Measured SNR was 21.2dB (Pre-FEC BER ~ 2e-7)
- Post-FEC BER was < 1e-15

Receiver Measurements



- Jitter Tolerance is measured at a BER of 1e-6
  - Below the KR4 FEC limit of ~2e-5

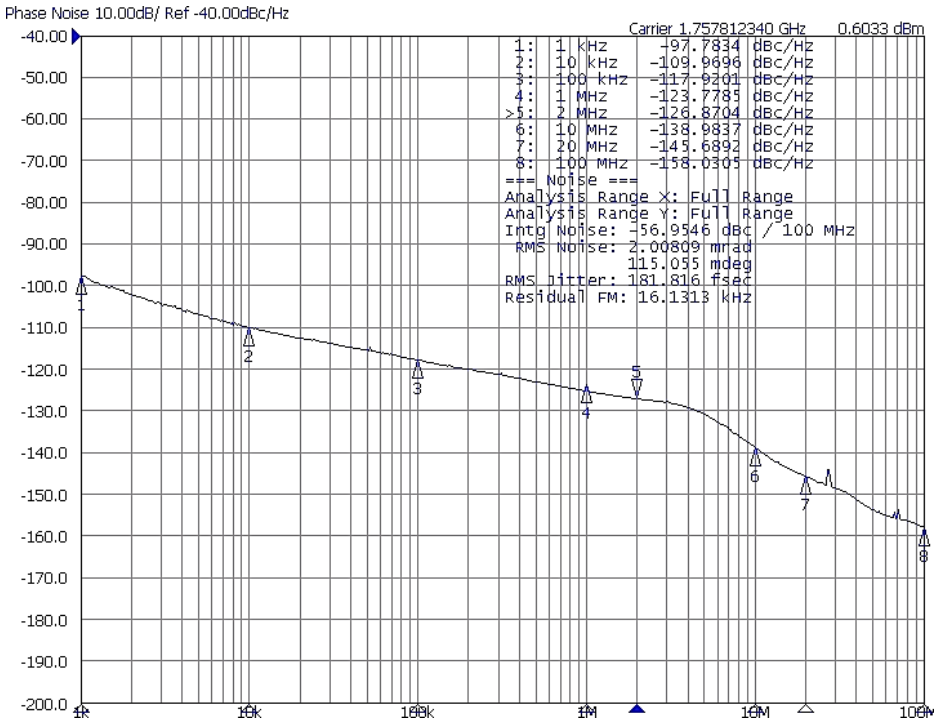
PLL Architecture



- Frac-N, LC, 2nd order Type-II with slow loop
- Multi modulus divider with smooth stage transitions
- Wide range output and programmability
  - Output frequency: 9.9~16 GHz, programmable Kvco
- Bandwidth control from ~30KHz to ~4MHz

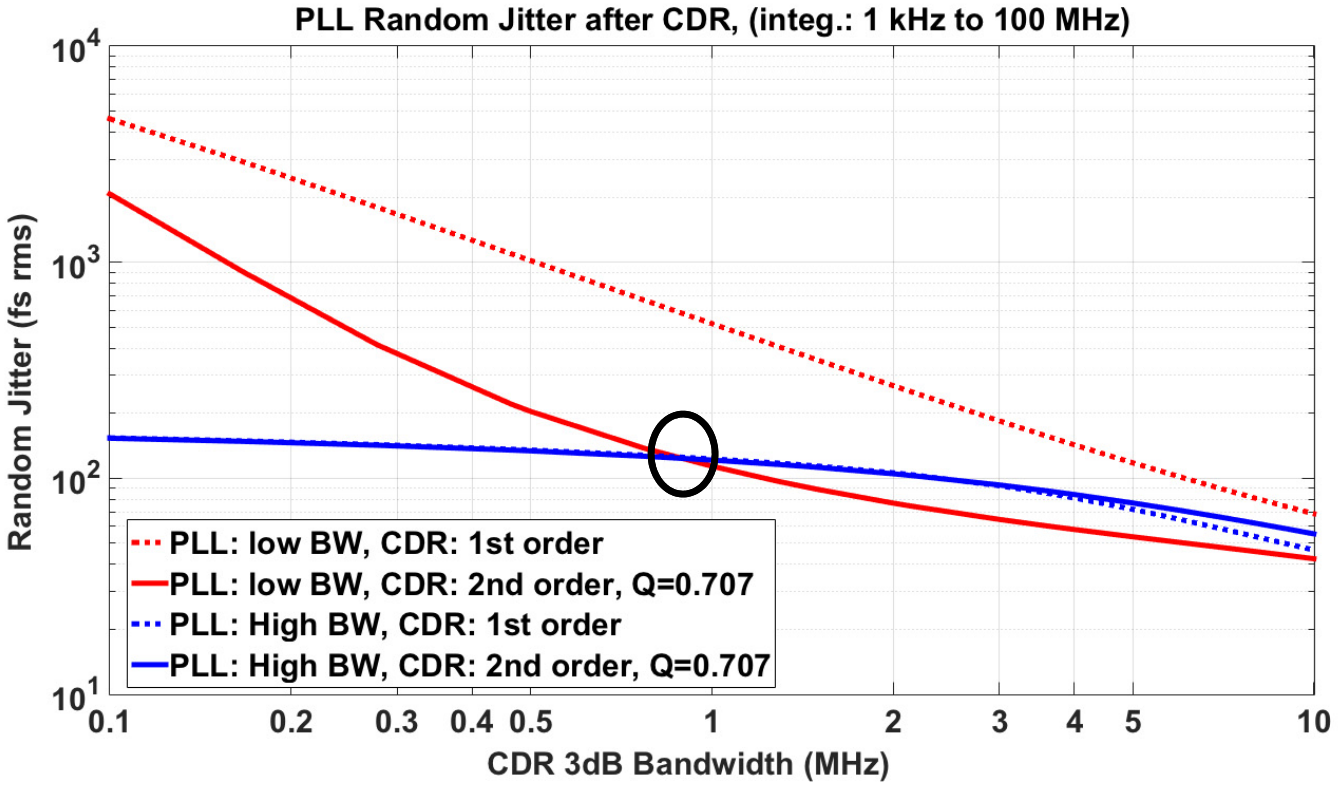
PLL Measurements

- Measured at TX o/p: 181 fs rms (1k~100MHz)
  - TX outputs with low frequency data pattern (1.7GHz)
  - Integer-N measurement with 625MHz clean refclk
  - Broadband integrated jitter (> 2Mhz) is 240fs rms

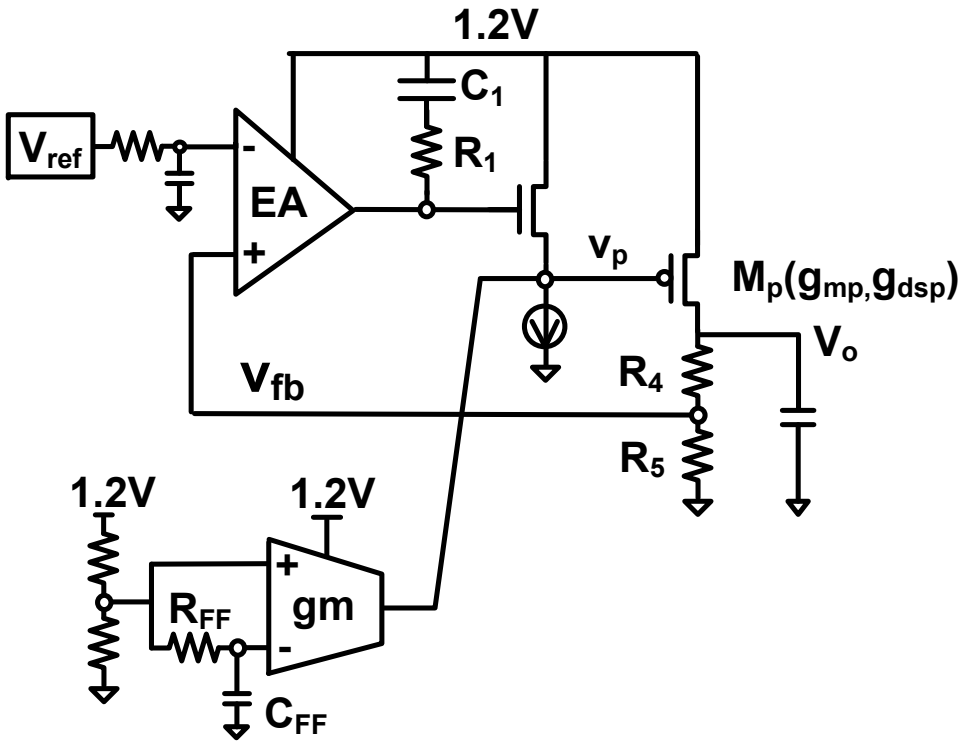


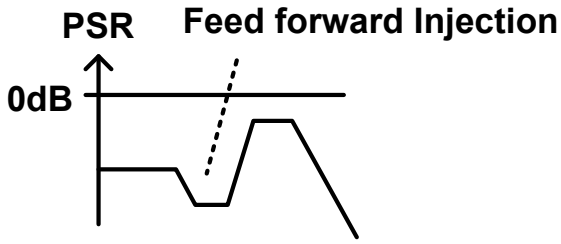
PLL Measurements

- Plot shows RJ measured after CDR high pass
  - X-axis is a sweep of the 3dB corner frequency
  - Measured raw phase noise used for calculation



Regulator Architecture





Ideal Injection at Vp = $V_{1.2}$(1 + g_{dsp}/g_{mp})*

- Feed-forward path provides notch around sensitive frequencies (switching regulator noise, PLL BW)
- Reduced on board requirements

Performance Summary

Performance Summary		
Max Data rate	32	Gbd
RX analog BW	18	Ghz (Typical)
AFE ENOB	5.7	@ 1Ghz
	4.9	@ Nyquist
Jitter tolerance	Exceeds VSR	Measured for NRZ
PPM tracking	< +/- 400	ppm w.r.t reference clk
Max TX swing	1400	mV differential peak-peak
NRZ skew control	+/- 1	UI
Skew resolution	100	fs
TX PLL RJ	181	fs rms (1 kHz - 100 MHz)
TX RJ	240	fs rms (> 2 MHz)
Supplies	1.2 / 0.9	Volts
Power	2.4	Watts for entire XCVR chip*
Chip dimension	6.3 x 4.9	mm
Technology	28nm	CMOS Logic

*Chip power with full bi-drectional 100G traffic

Conclusions

- The PAM-4 Ethernet XCVR enables 100Gb/s over reduced optical components
- The chip shows error free operation at 50Gb/s/link over existing backplane channels with a KR4 FEC
- Provides pathway to 50, 200 and 400Gb/s as recognized by the standards
- Low power to support QSFP applications

Acknowledgements

- The authors would like to thank the layout team for their efforts and the system hardware team for all measurements

A 56Gb/s NRZ-Electrical 247mW/lane Serial-Link Transceiver in 28-nm CMOS

Takayuki Shibasaki[1], Takumi Danjo[1], Yuuki Ogata[1], Yasufumi Sakai[1], Hiroki Miyaoka[2], Futoshi Terasawa[2], Masahiro Kudo[2], Hideki Kano[2], Atsushi Matsuda[2], Shigeaki Kawai[2], Tomoyuki Arai[2], Hirohito Higashi[2], Naoaki Naka[2], Hisakatsu Yamaguchi[1], Toshihiko Mori[1], Yoichi Koyanagi[1], and Hirotaka Tamura[1]

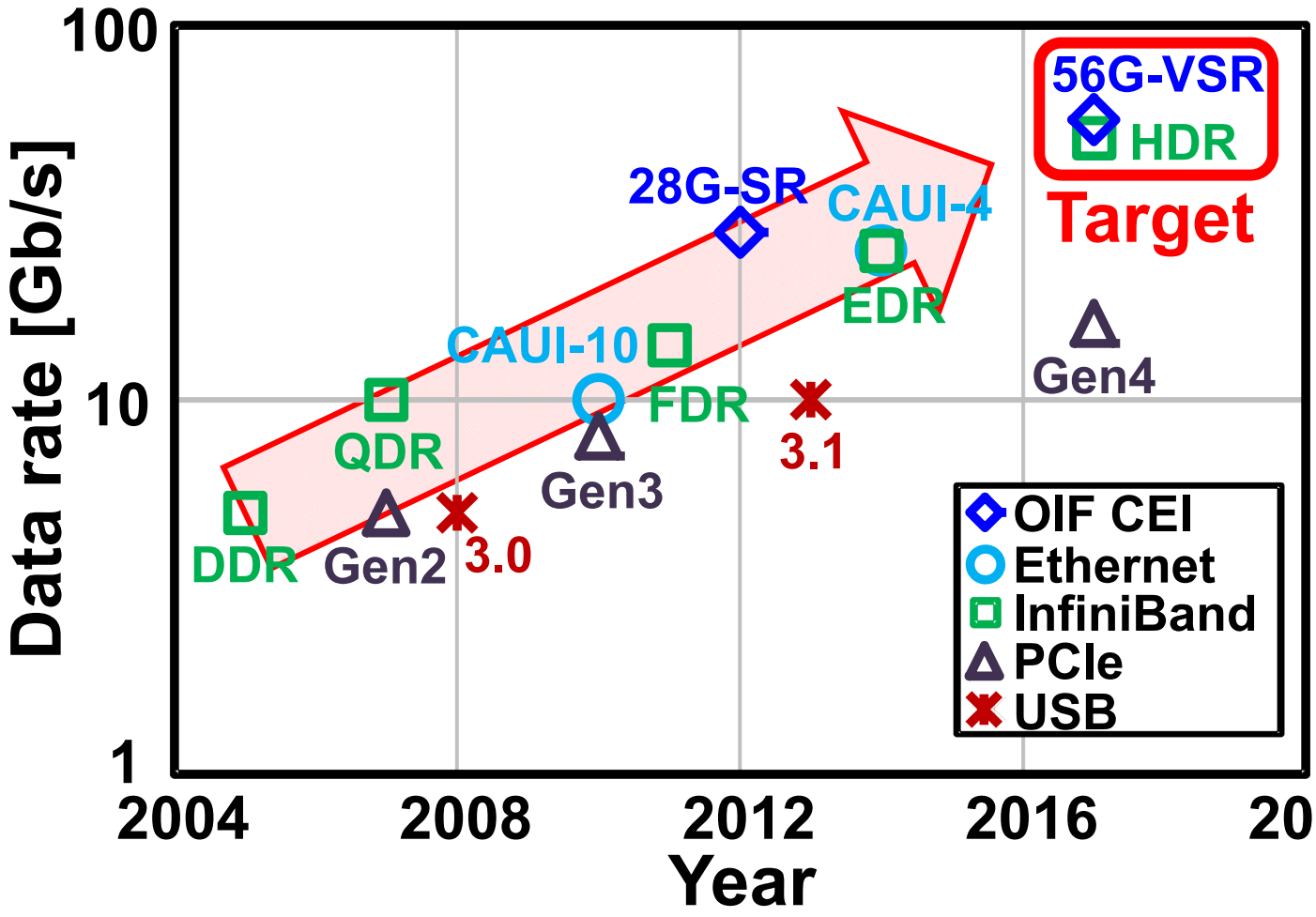
1. Fujitsu Laboratories, Japan
2. Socionext, Japan

Outline

- Motivation
- Receiver design
  - Phase detection
  - Look-ahead DFE selector
  - Eye monitor
- Transceiver design
- Measurement results
- Summary

Wireline Data-Rate Trend

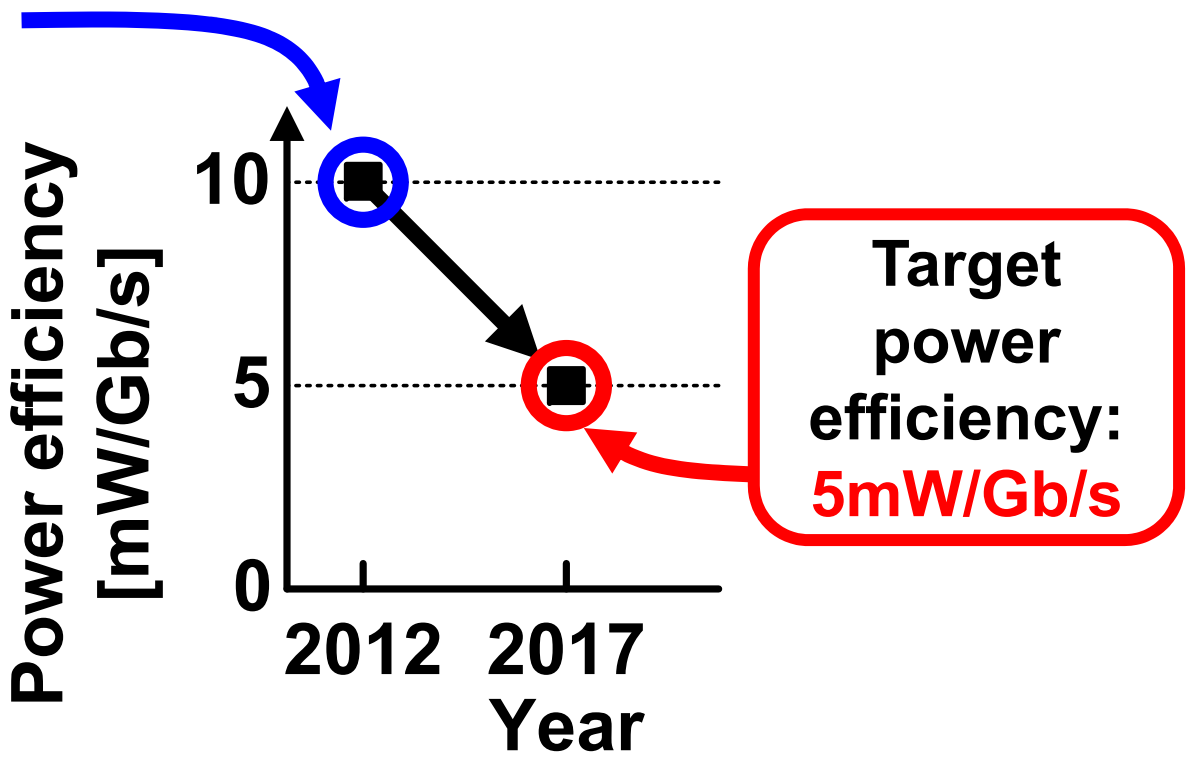
- With rapid growth of data traffic in data centers, data rates over 50Gb/s will be required



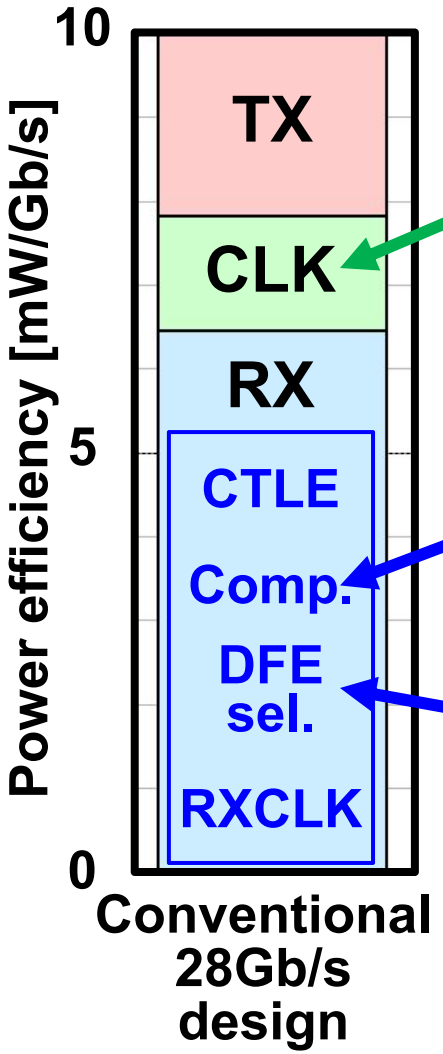
Target channel loss is 18dB@28GHz

Motivation

- Transceiver power consumption should not increase to meet the data center power supply limitation
- Power efficiency of conventional 28Gb/s transceiver is around 10mW/Gb/s

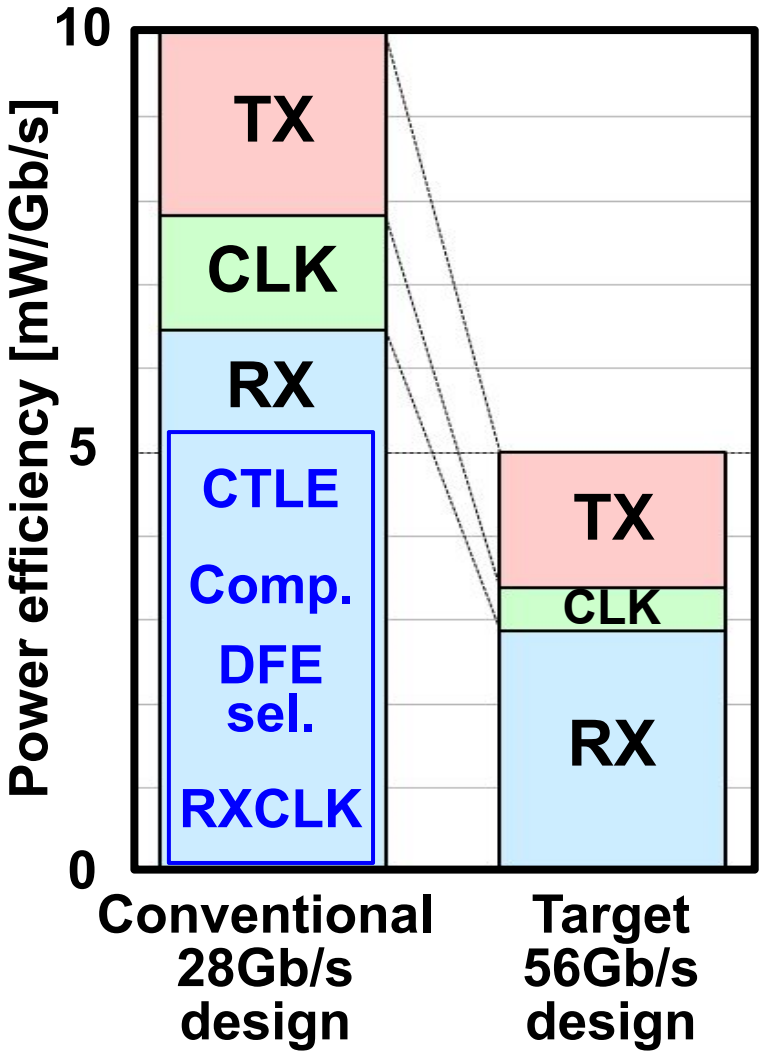


Technical Challenges



- **Number of sampling phases**
  - 2x sampling doubles clock phase
    - Clocking power ↑
- **Number of comparators**
  - Front-end power scales with the number of comparators
    - CTLE, Comp., & RXCLK power ↑
- **DFE selector speed**
  - Sufficient BW needed
    - DFE selector power ↑

Solutions



- **Number of sampling phases**
  - **Baud-rate sampling PD**
    - PLL & CDIST power : 1/2
- **Number of comparators**
  - **Detect phase from sampled data to reduce the # of comps.**
  - **1 comparator eye monitor**
    - CTLE & RXCLK power : 2/3
- **DFE selector speed**
  - **Look ahead DFE selector relax operating speed**
    - DFE selector power : 1/2

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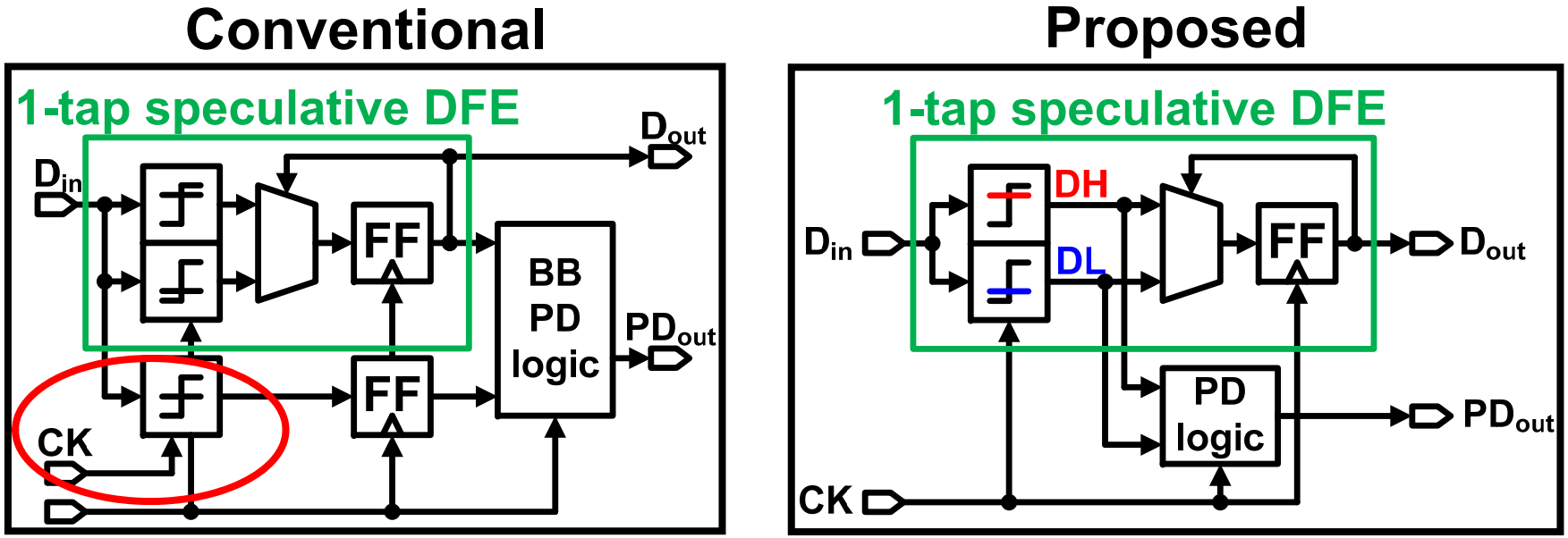
Phase Detection Scheme

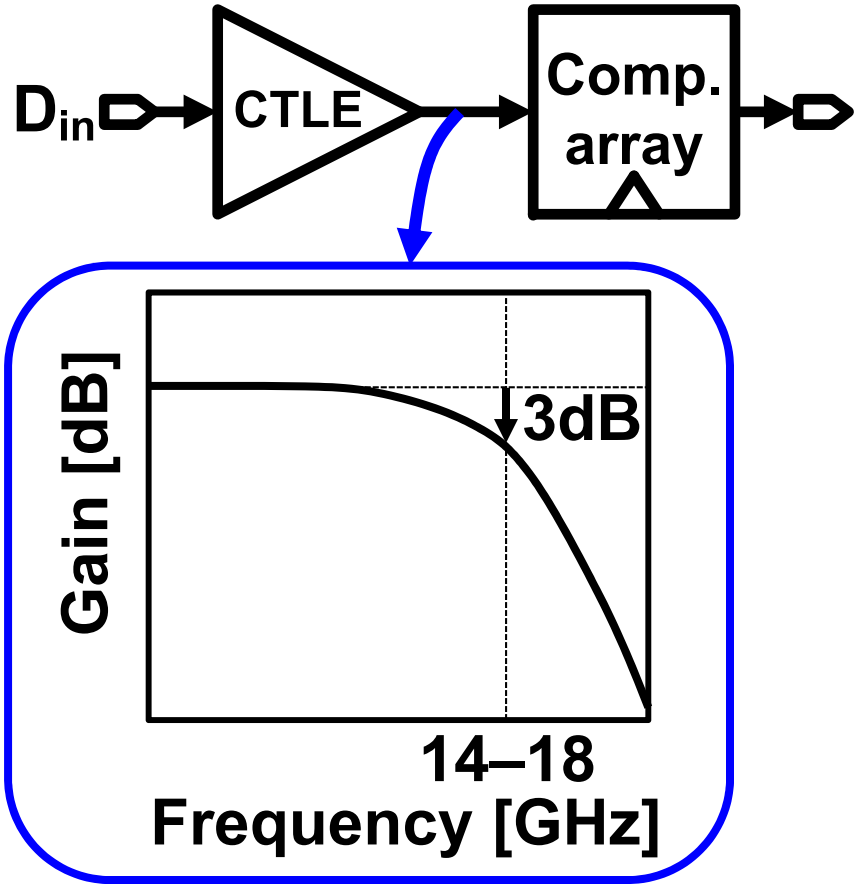
- Detect phase from 1-tap speculative DFE data

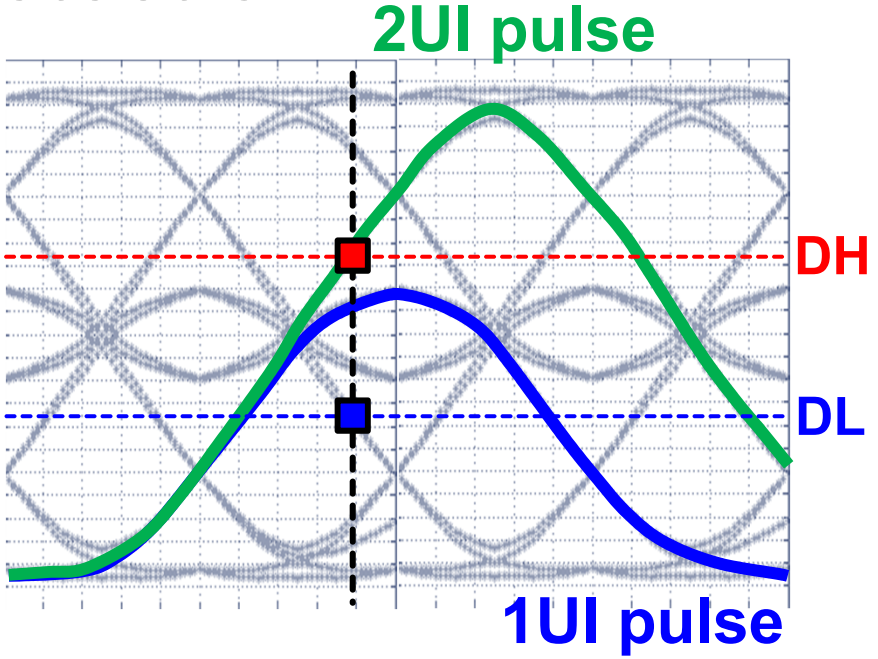


  - Number of comparators is 2/3
  - Number of clock phases is 1/2
    - PLL and clock distribution power is 1/2

Target Frequency Characteristics

- f_{3dB} at CTLE output is adjusted between 14–18GHz for phase detection

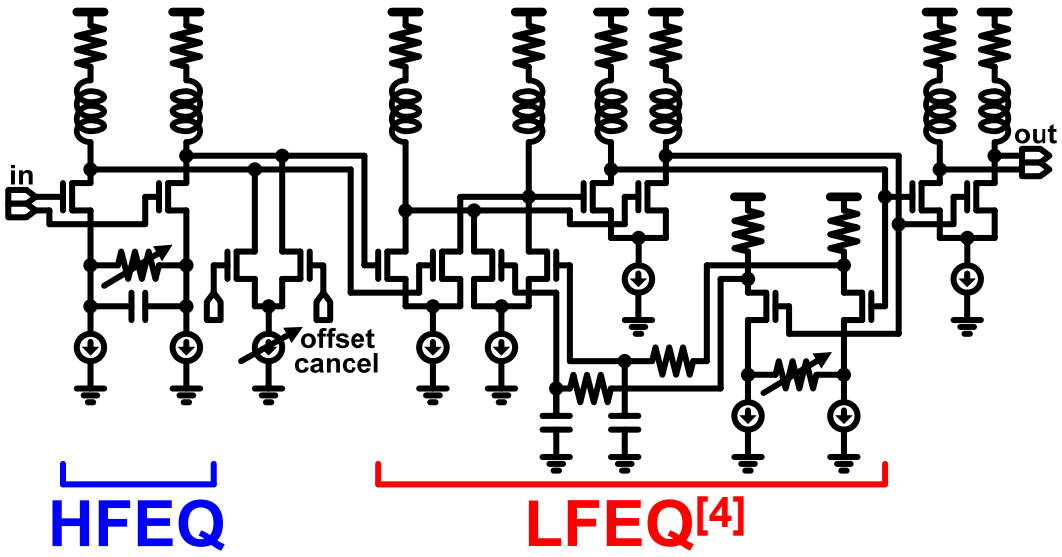


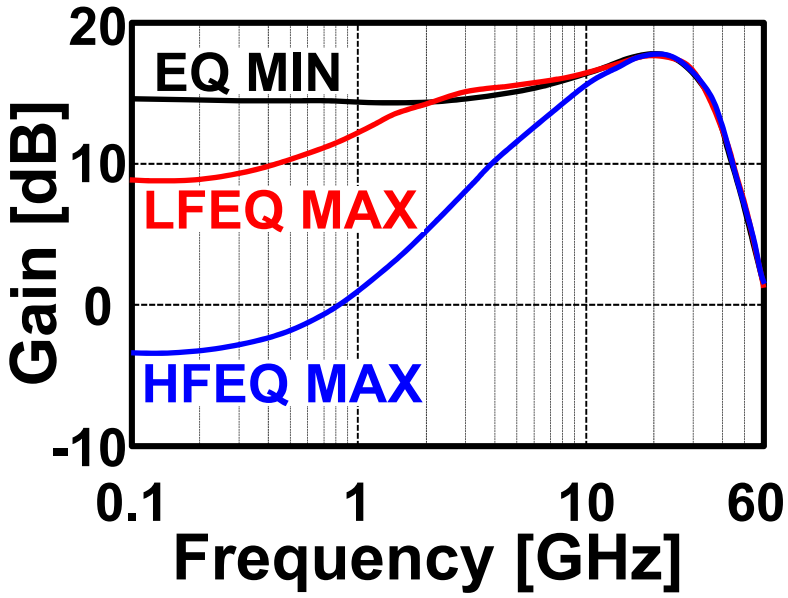


2UI pulse swing reaches full swing at this frequency characteristic

CTLE Design

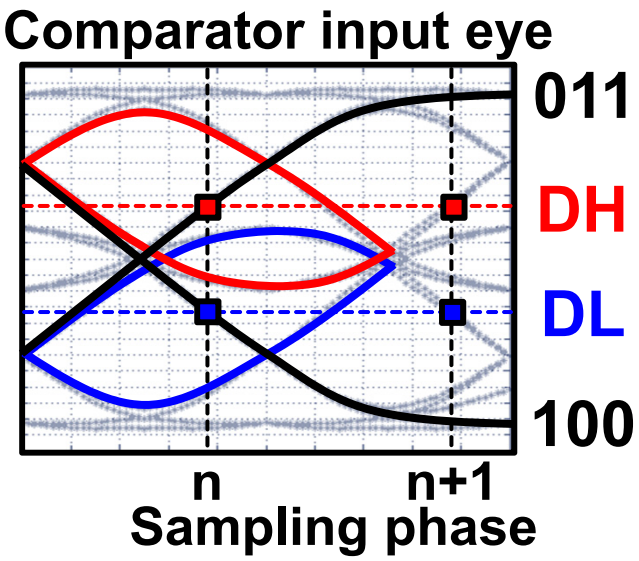
- Achieved enough performance with same power consumption
  - BW_{-3dB} = 34GHz, G_{DC} = 14dB

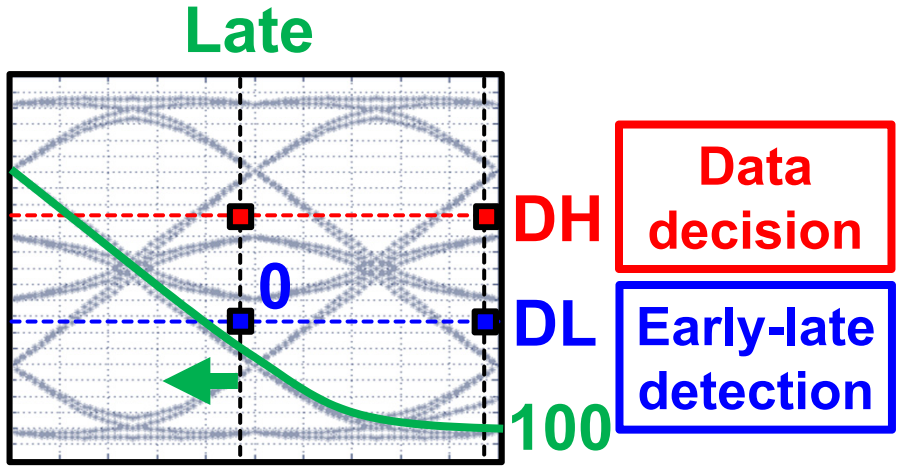


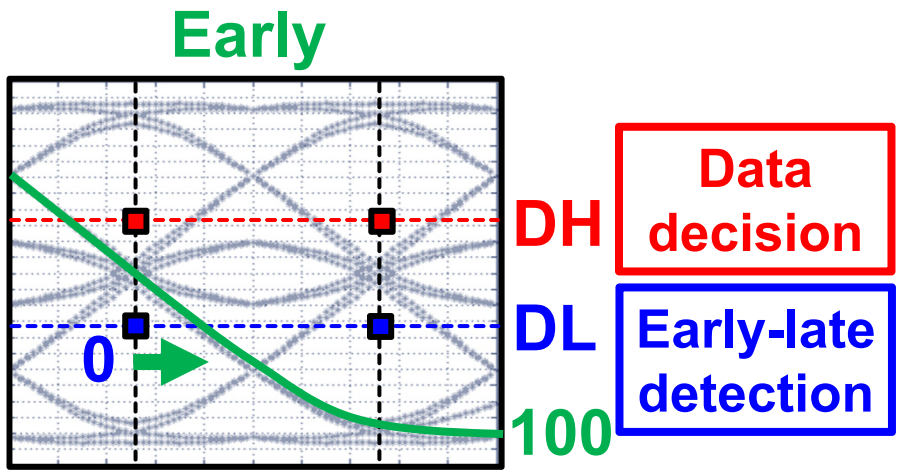


[4] S. Parikh, et al., "A 32Gb/s Wireline Receiver with a Low-Frequency Equalizer, CTLE and 2-Tap DFE in 28nm CMOS," ISSCC 2013.

Phase Detector Operation

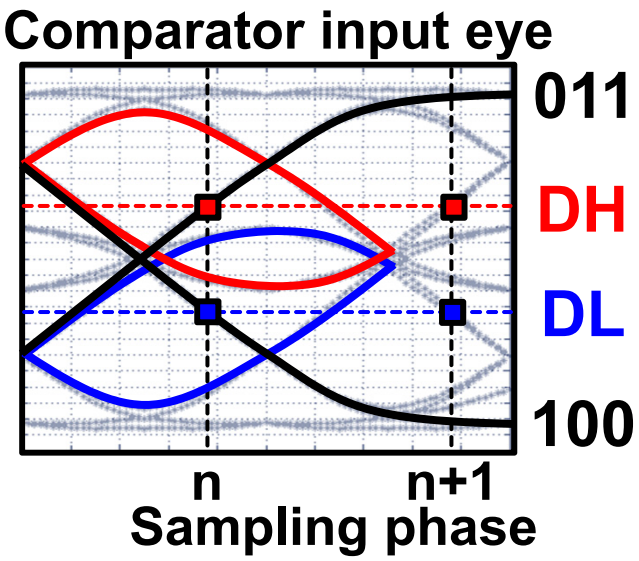


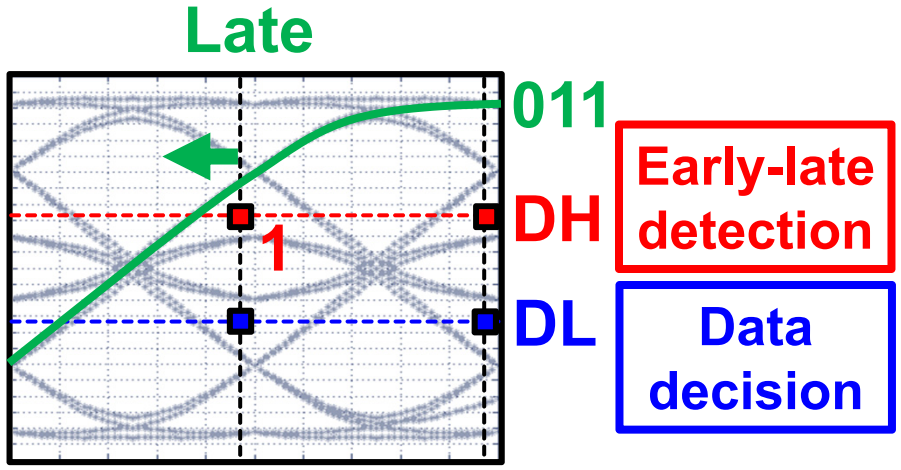


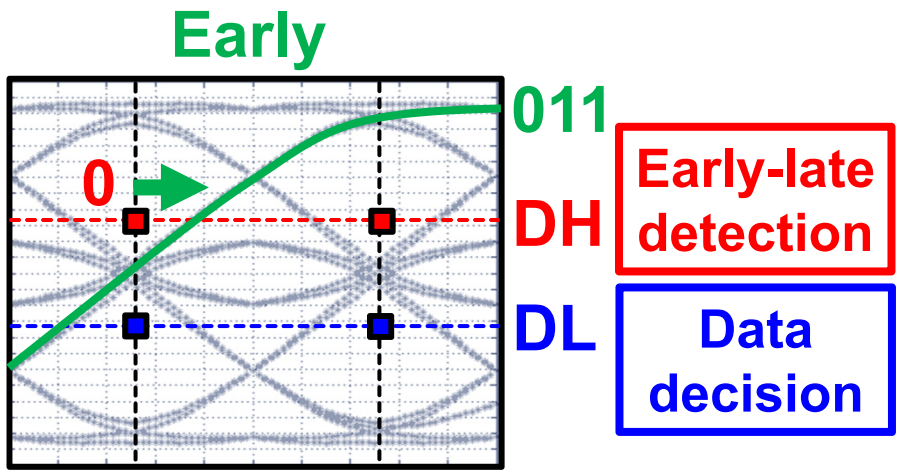


DH			DL			UP/DN [1:0]
n−1	n	n+1	n−1	n	n+1	
0	1	1	0	1	1	UP
	0					DN
1	0	0	1	0	0	UP
				1		DN
Other						Stay

Phase Detector Operation



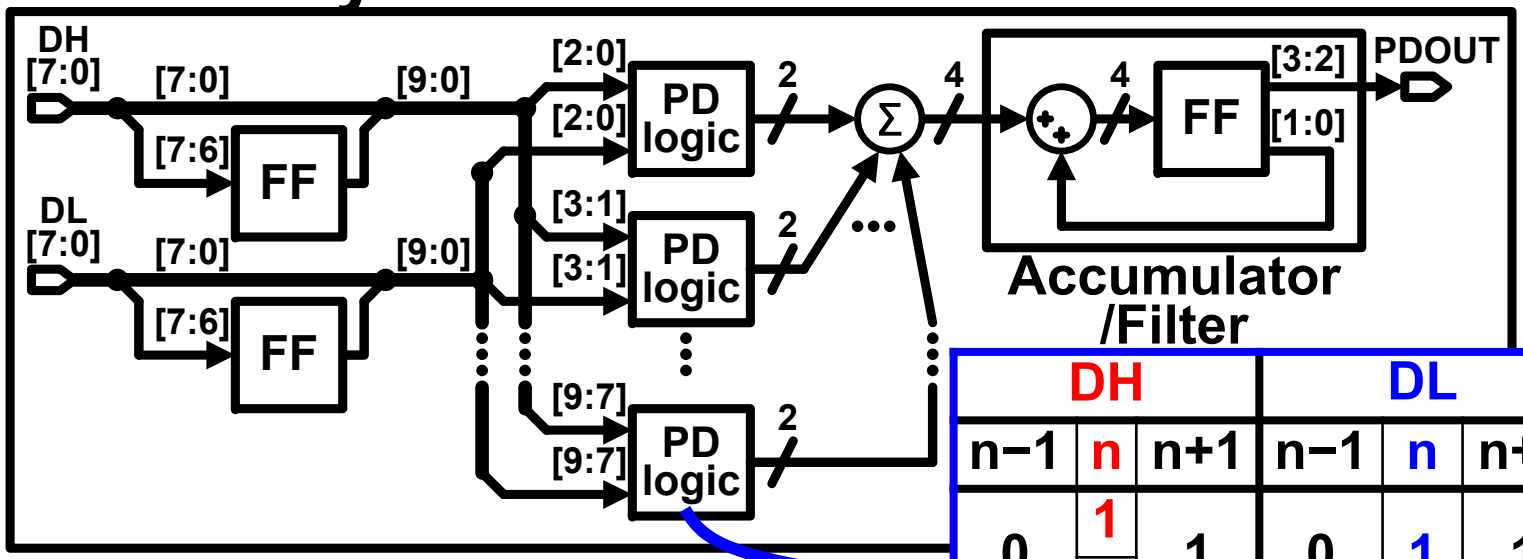




DH			DL			UP/DN [1:0]
n−1	n	n+1	n−1	n	n+1	
0	1	1	0	1	1	UP
	0					DN
1	0	0	1	0	0	UP
				1		DN
Other						Stay

Phase Detection Logic

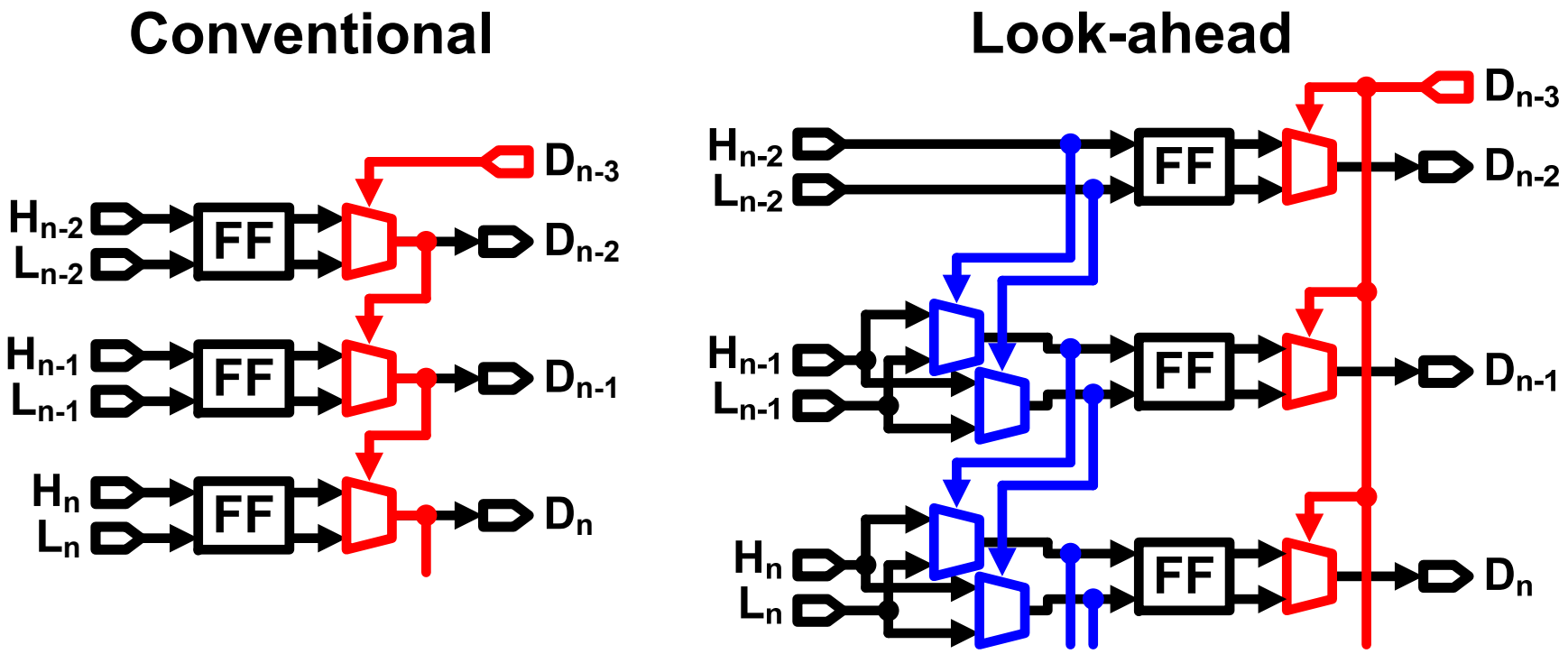
- Implemented in 7-GHz clock domain not to increase CDR loop latency
  - Latency of this block is 40UI



DH			DL			UP/DN [1:0]
n−1	n	n+1	n−1	n	n+1	
0	1	1	0	1	1	UP
	0					DN
1	0	0	1	0	0	UP
				1		DN
Other						Stay

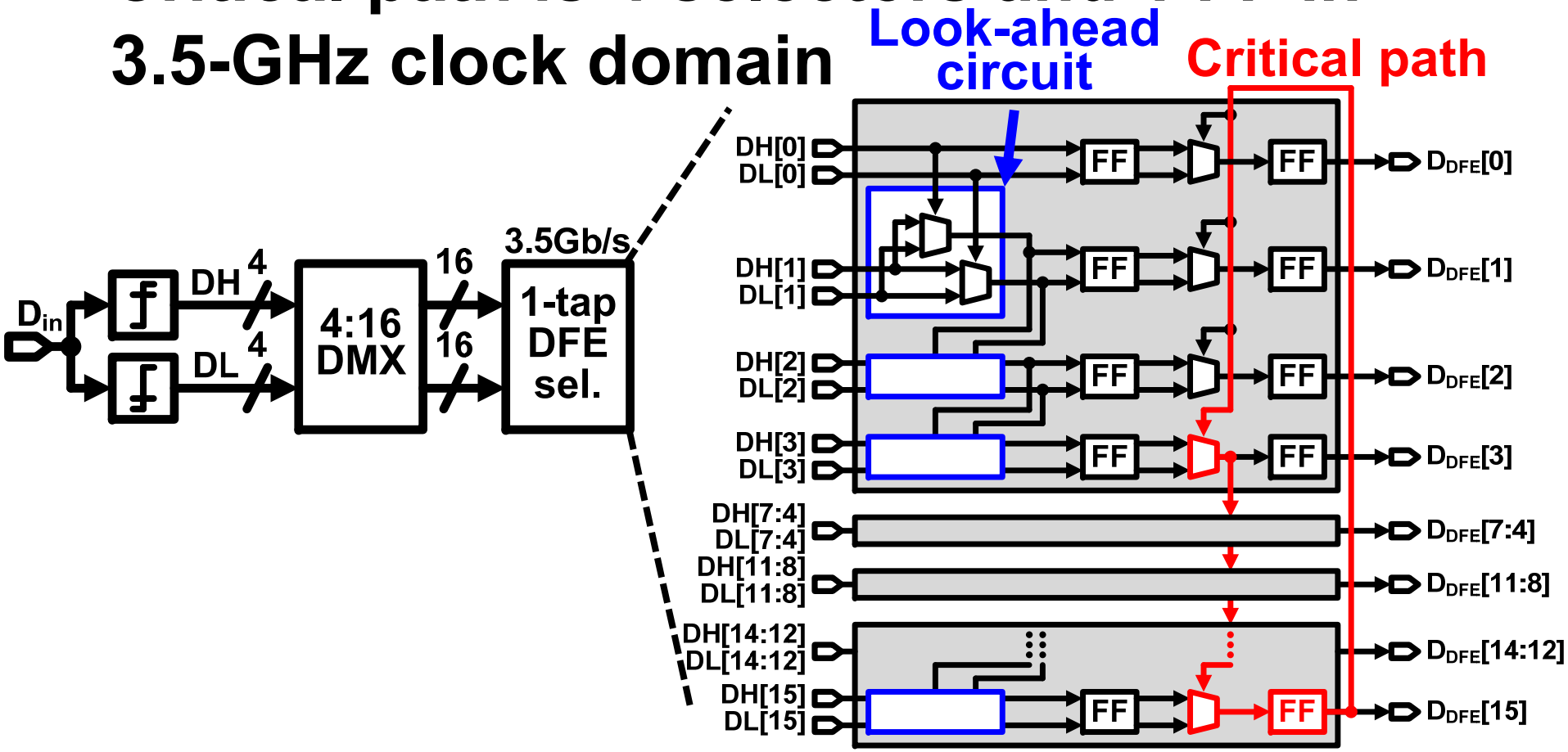
Look-Ahead Selection Scheme

- Look-ahead eliminates selector-output propagation



Look-Ahead 1-tap DFE Selector[1]

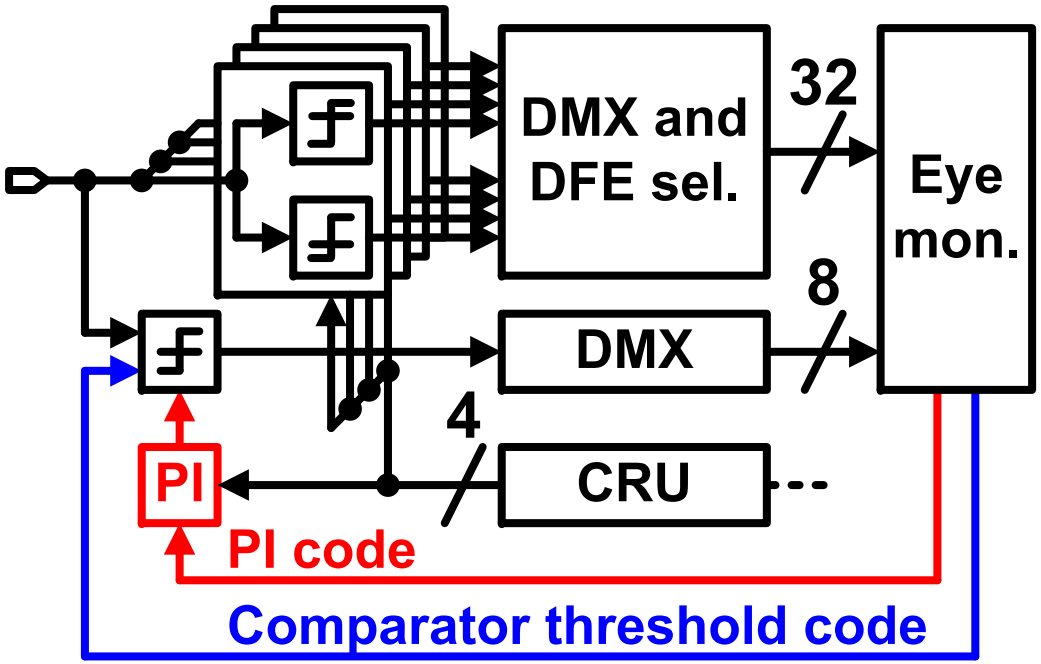
- Critical path is 4 selectors and 1 FF in 3.5-GHz clock domain

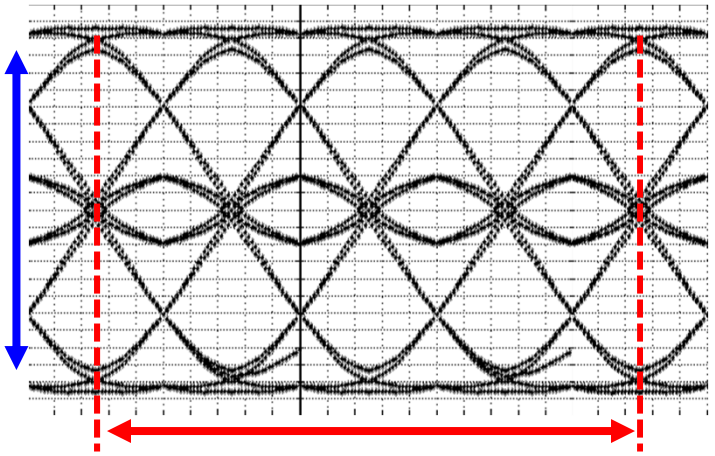


[1] T. Shibasaki, et al., "A 56-Gb/s Receiver Front-End with a CTLE and 1-Tap DFE in 20-nm CMOS," VLSI 2014.

Eye Monitor

- 1 comparator is used for eye monitoring
  - Sweep PI code and comp. V_{th}
  - DFE operation is considered for BER check





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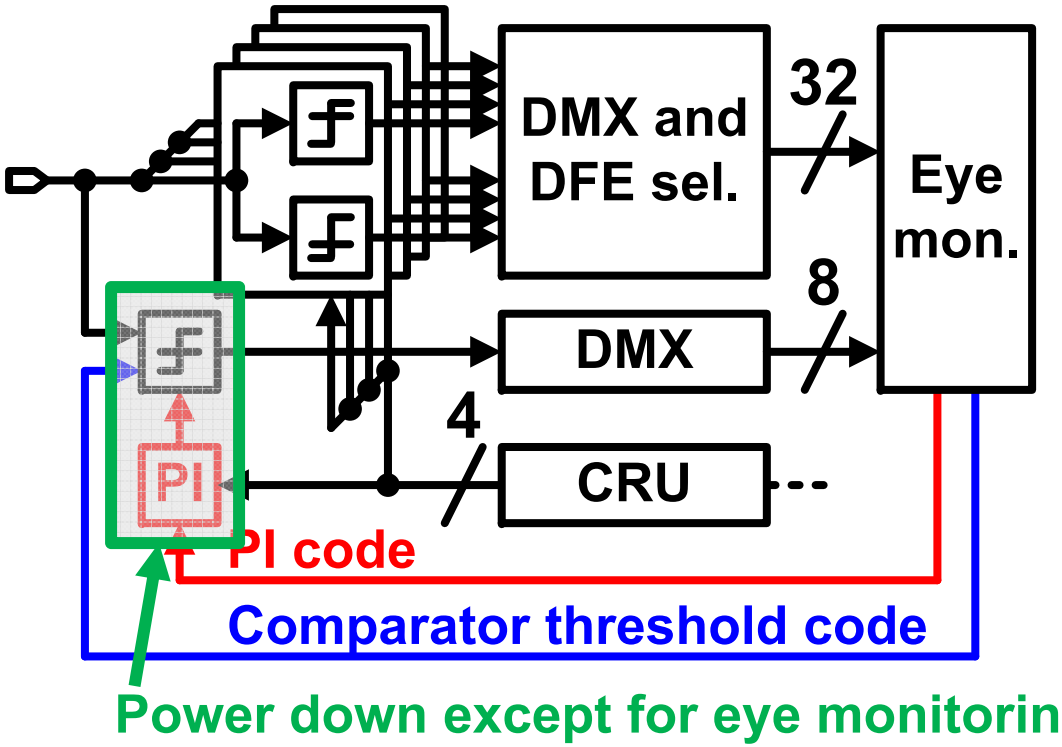

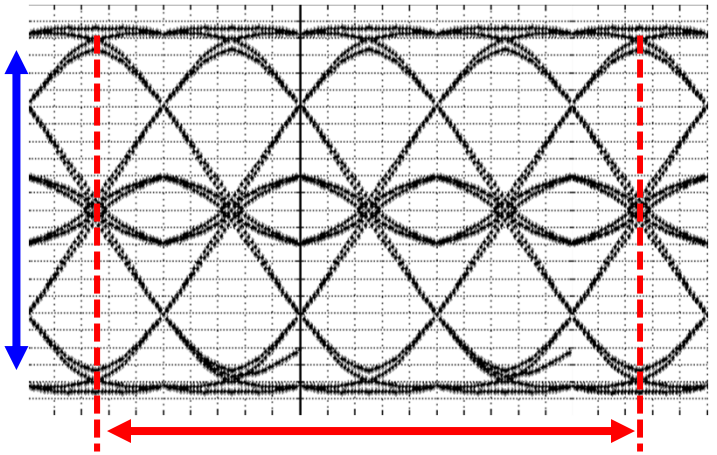

PI sweep the phase
from 0UI to 4UI

Outline

- Motivation
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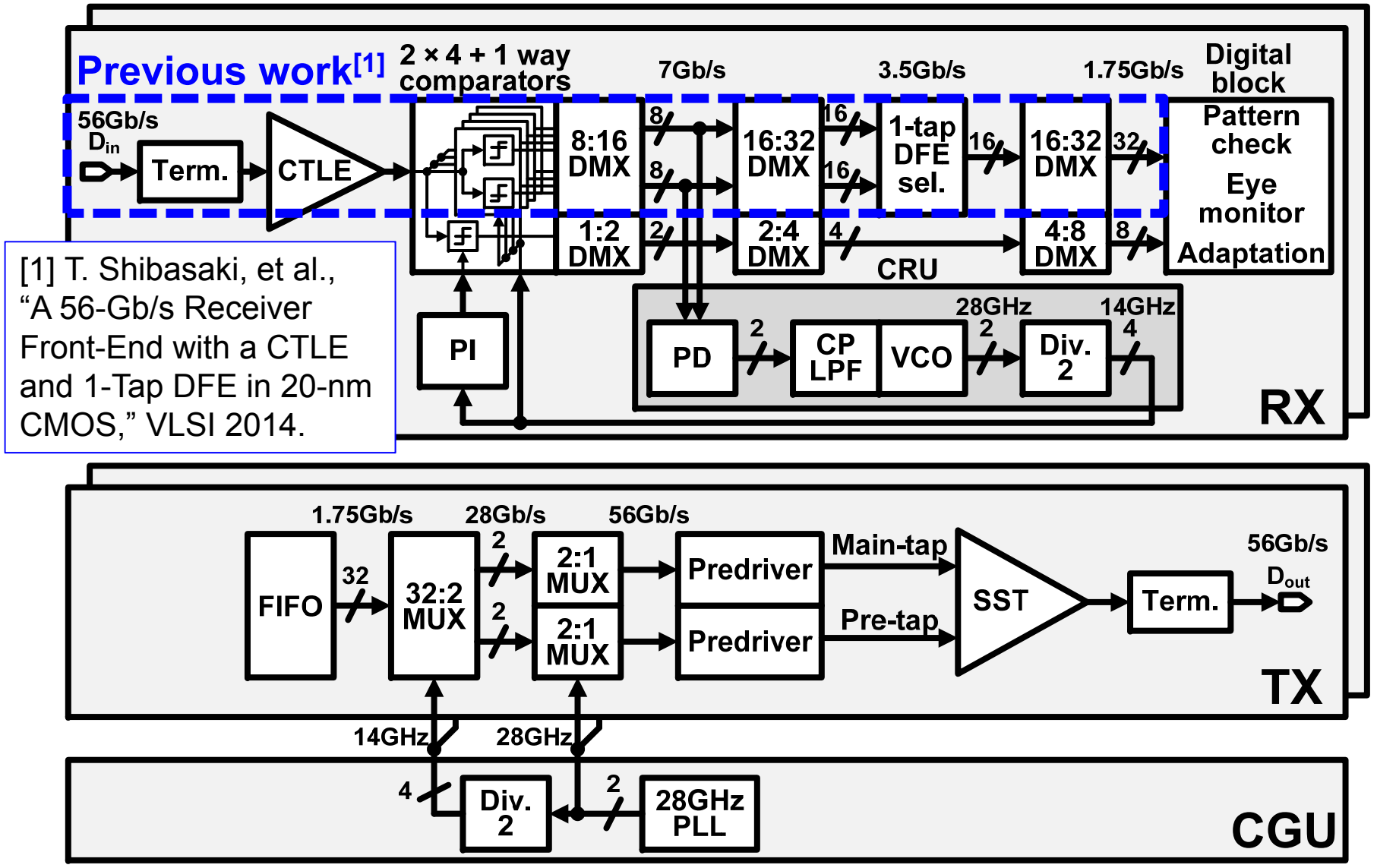
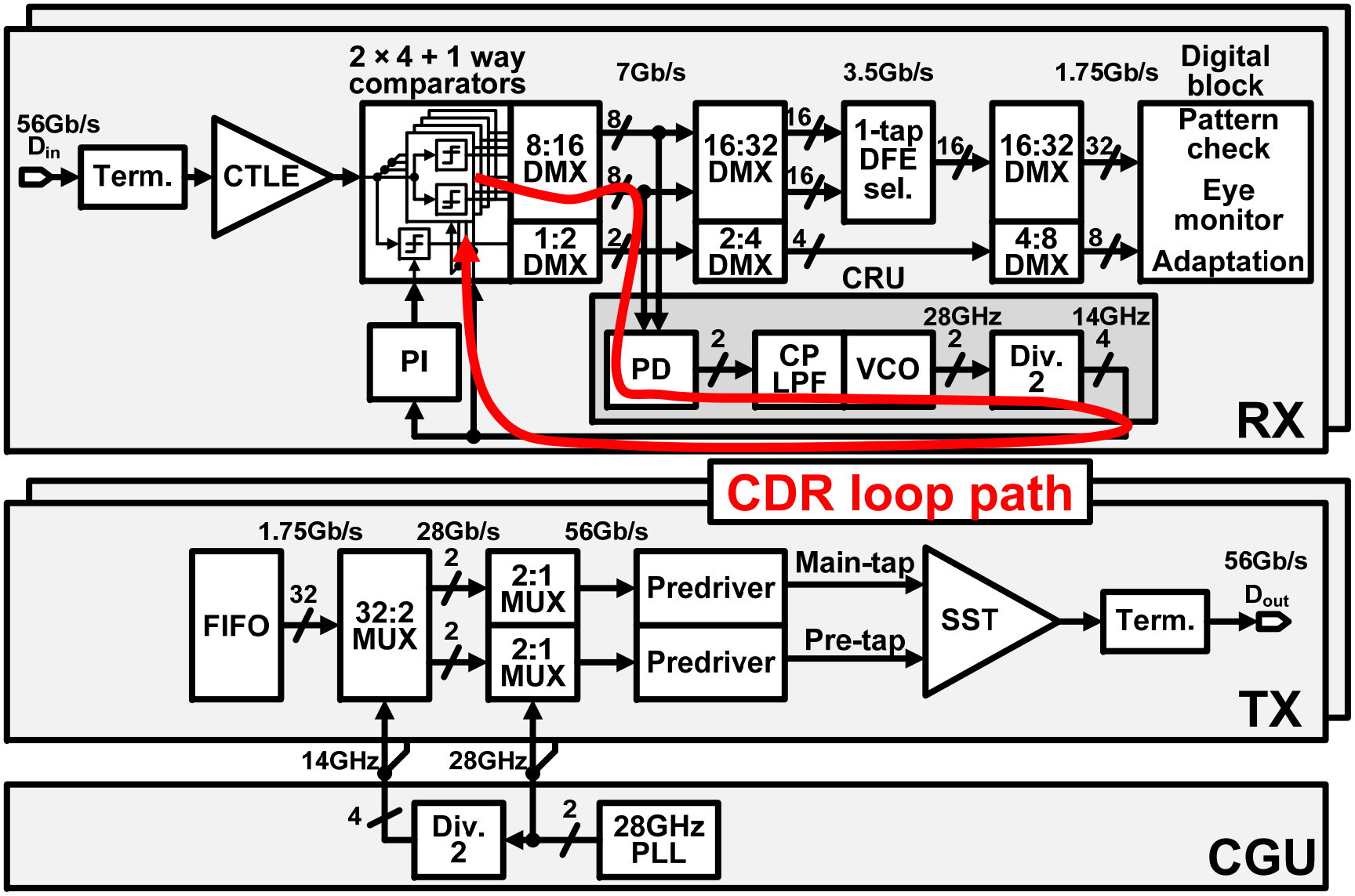
  - Look-ahead DFE selector
  - Eye monitor
- **Transceiver design**
- **Measurement results**
- **Summary**

Transceiver Design



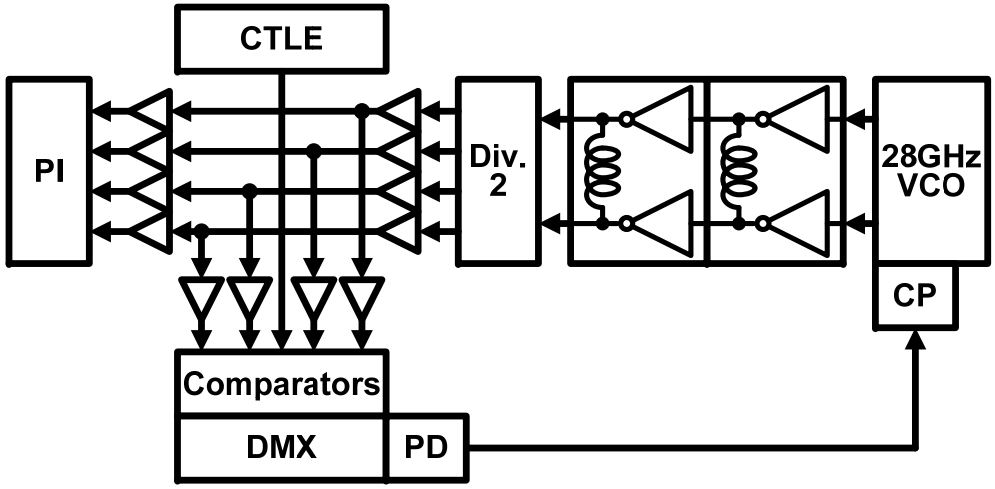
[1] T. Shibasaki, et al., "A 56-Gb/s Receiver Front-End with a CTLE and 1-Tap DFE in 20-nm CMOS," VLSI 2014.

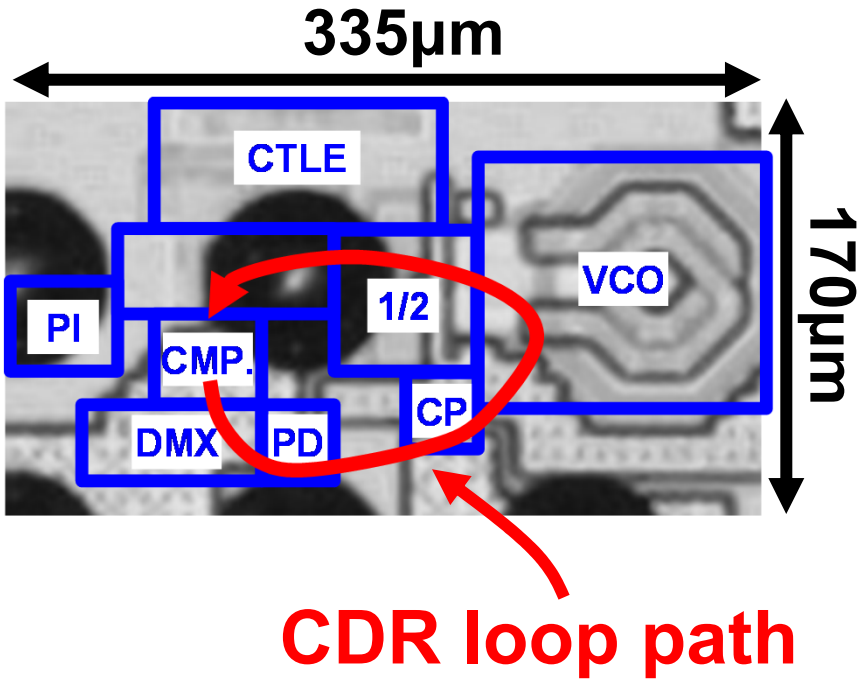
Transceiver Design



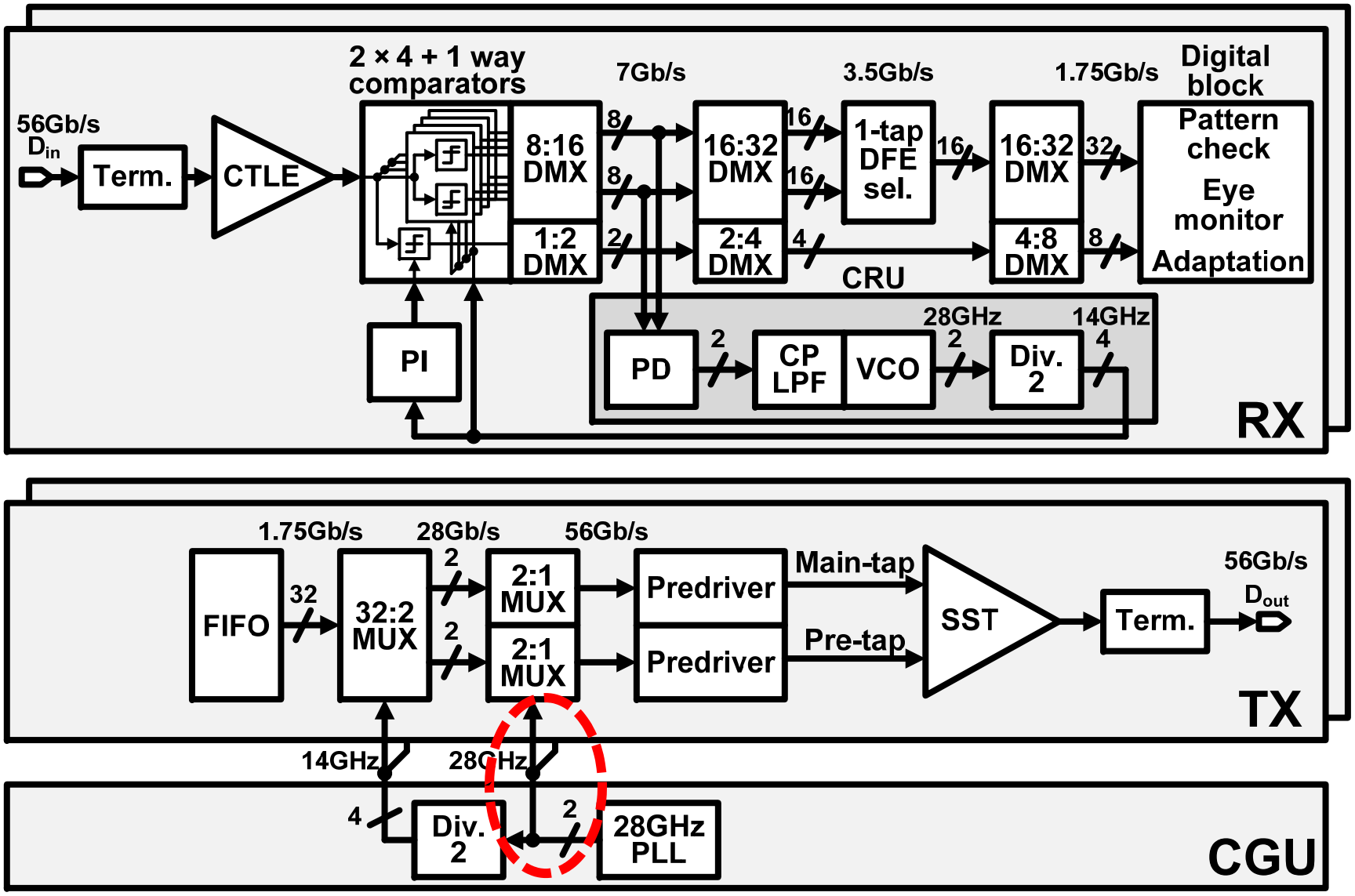
CDR Loop Path Design

- 28GHz clock path and CDR loop path are minimized



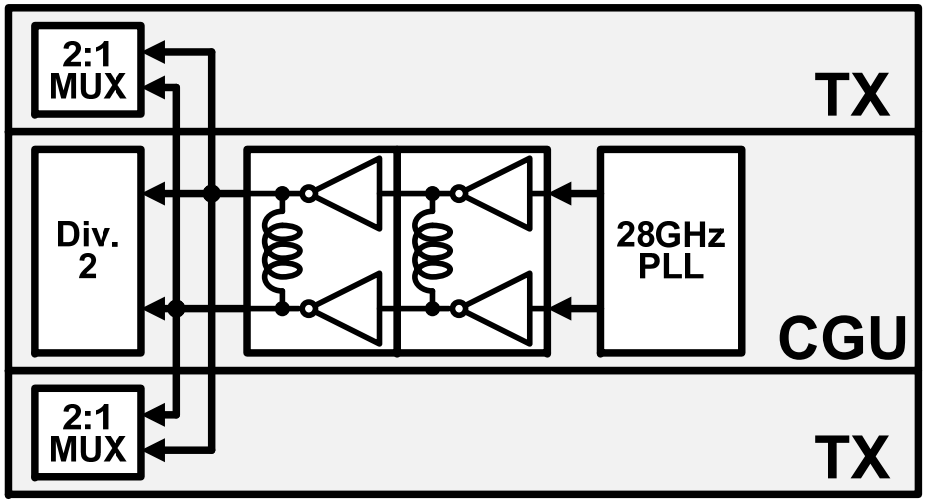


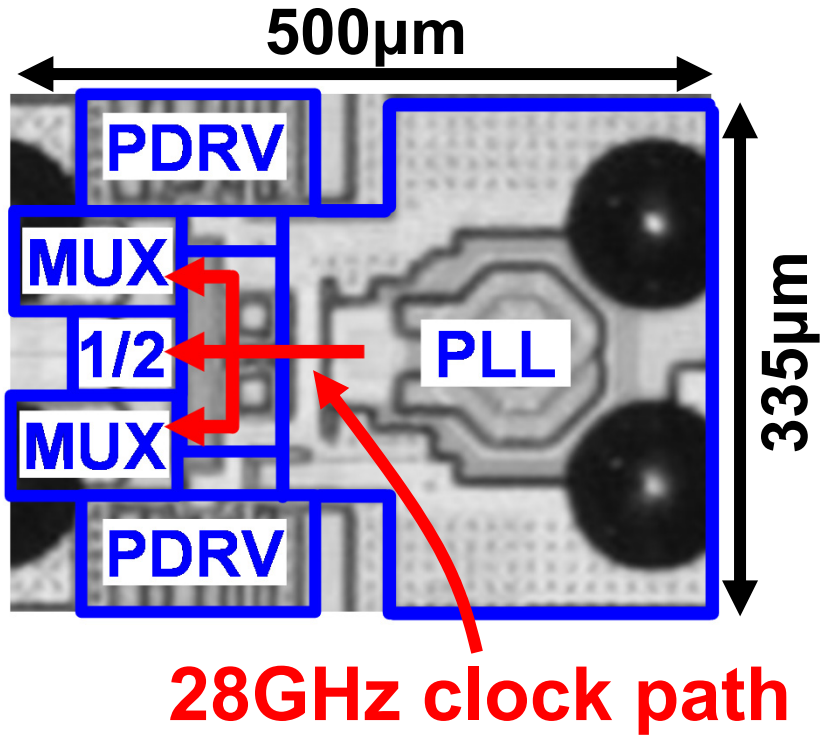
Transceiver Design



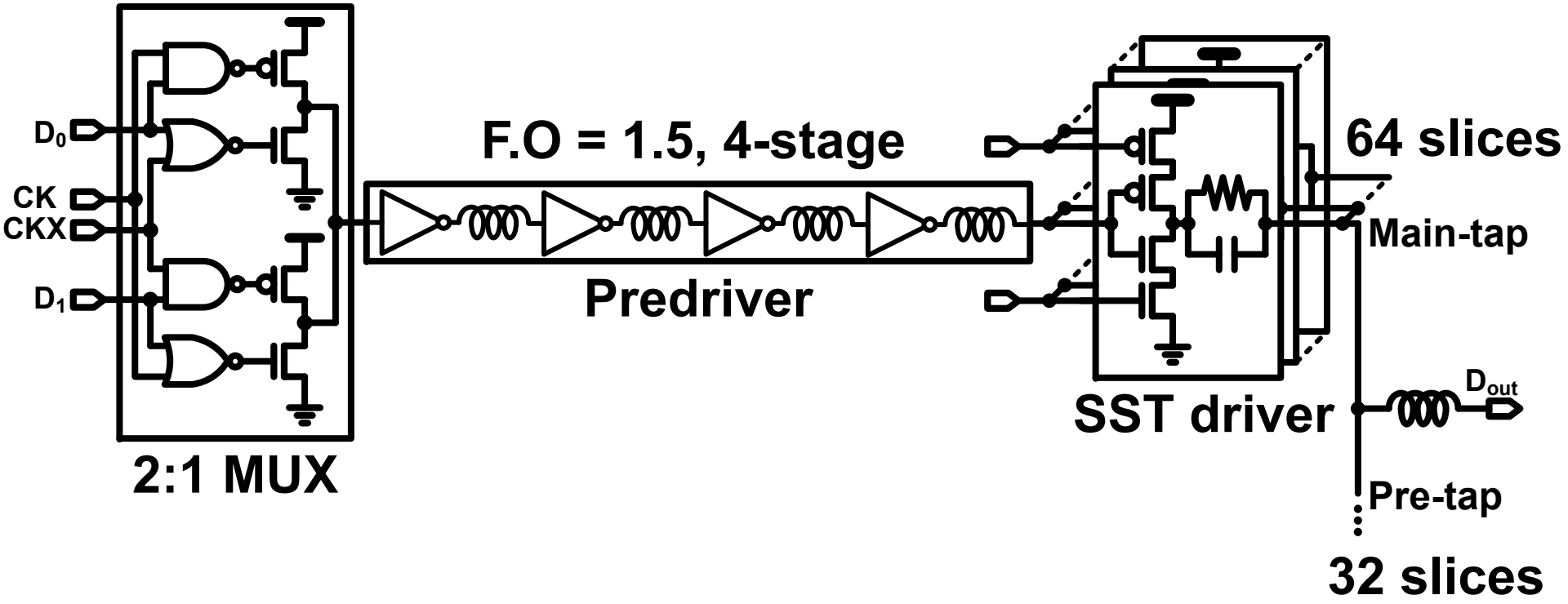
Transmitter Clock Path Design

- 2-stage narrow band buffer drives 2-lane 2:1 MUXs and divider
- 28GHz clock path is minimized





Transmitter Front-end Design



Outline

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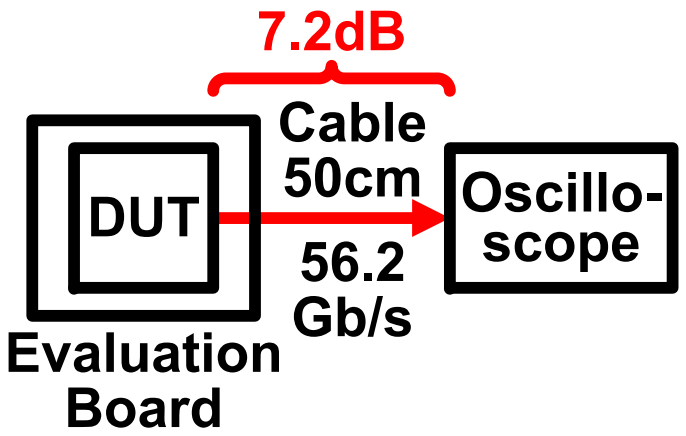
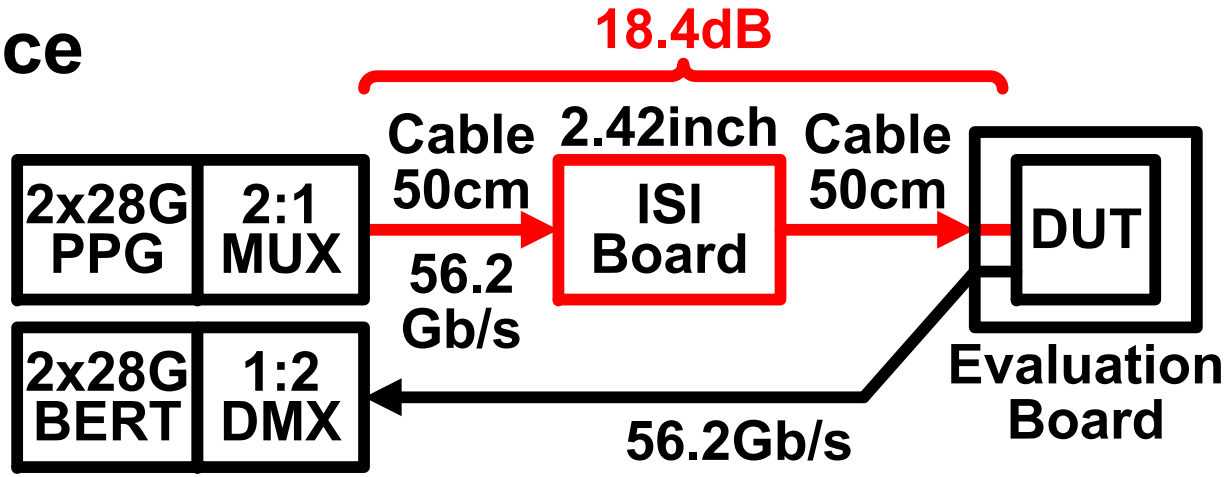
  - Look-ahead DFE selector
  - Eye monitor
- Transceiver design
- **Measurement results**
- **Summary**

Measurement Setup

- **TX setup**
  - Eye diagram

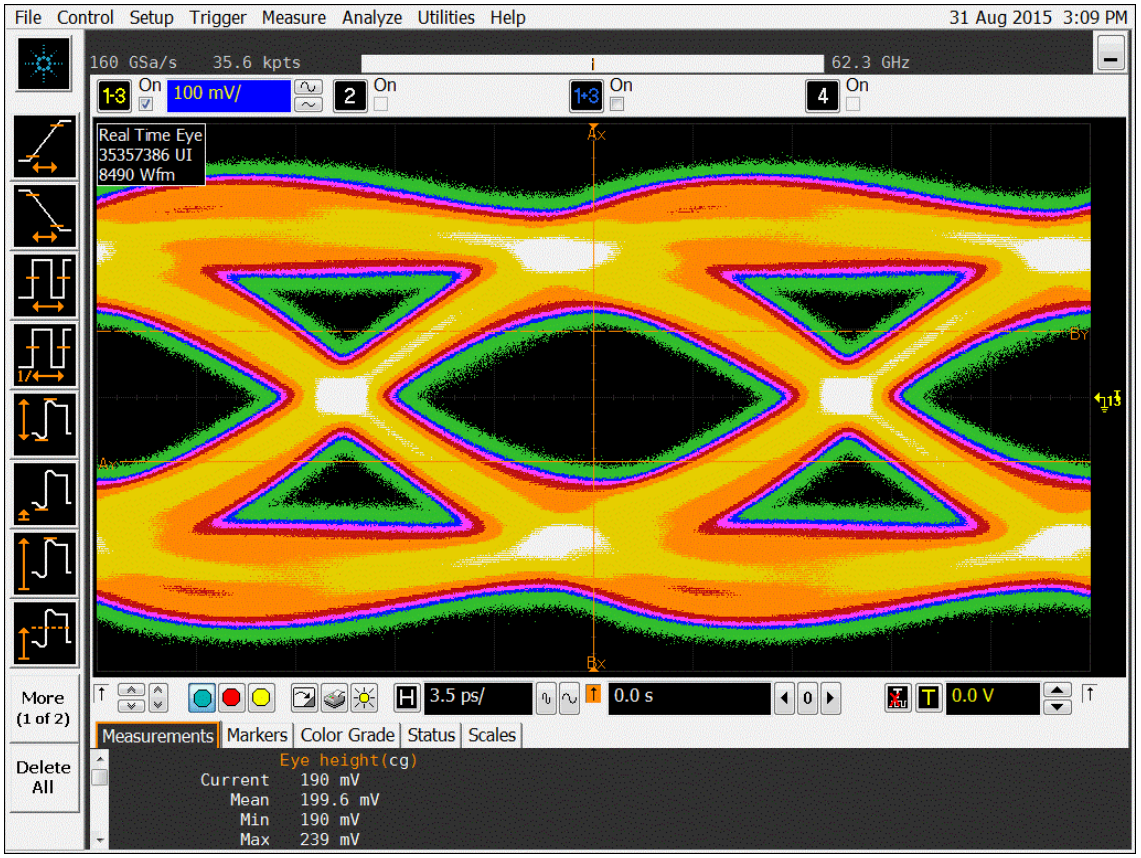


- **RX setup**
  - Jitter tolerance
  - Internal eye diagram



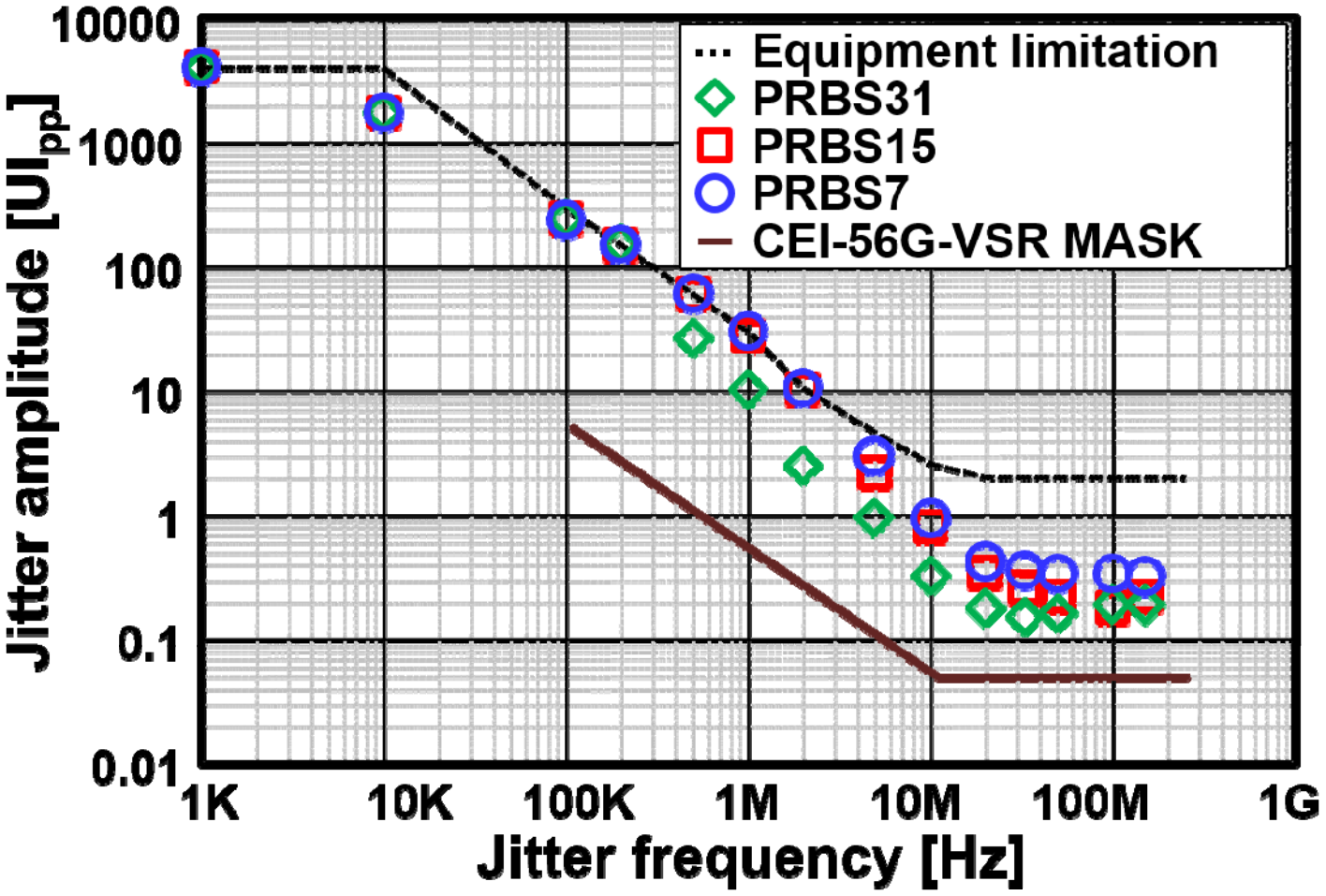
Transmitter Eye Diagram

- 56.2Gb/s, PRBS15, 7.2dB loss at 28.1GHz
- T_j = 8.8ps @BER of 10^{-15}



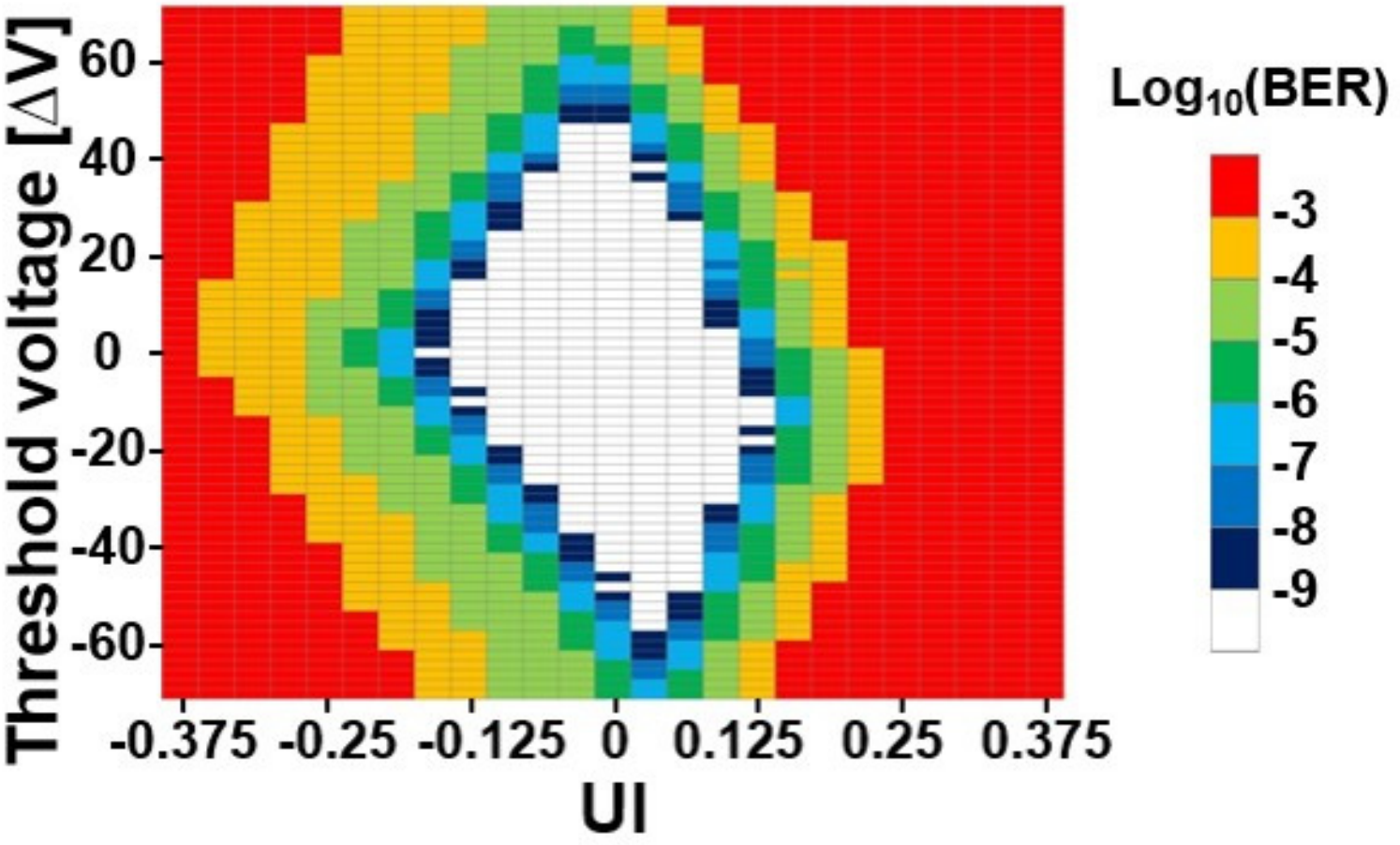
Receiver Jitter Tolerance

- 56.2Gb/s, BER = 10^{-12}



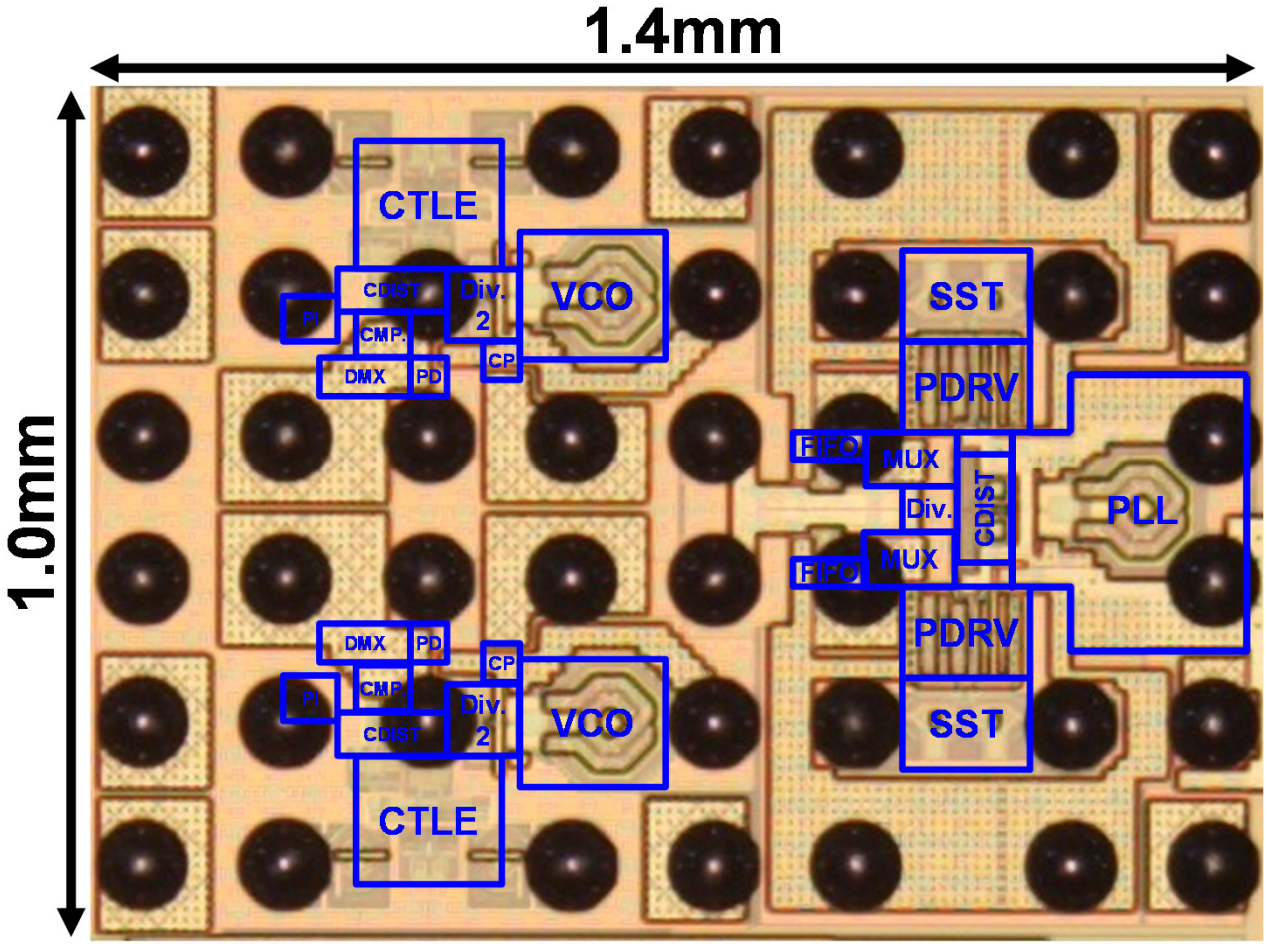
Receiver Internal Eye Diagram

- 56.2Gb/s, PRBS15, BER = 10^{-9}



Chip Photograph

56.2Gb/s 2-lane Transceiver



Performance Summary

	T. Shibasaki VLSI 2014	J. Lee VLSI 2015	J. Han VLSI 2015	This work
Data rate [Gb/s]	56	55.5-56.5	60	56.2
Technology	20-nm CMOS	40-nm CMOS	65-nm CMOS	28-nm CMOS
Power [mW/Gb/s]	RX: 3.16	TX: 8.00 RX: 3.93	RX: 2.88	TX: 1.87 RX: 2.53
Supply voltage [V]	0.9	1.2	1.2/1.0	0.96
Channel loss [dB]	23	–	–	18.4
Area [mm^2]	RX: 0.34	TX: 2.10 RX: 1.10	RX: 0.16	1.40 (2 lane)
TX function	–	4:1 MUX 60GHz PLL PRBS	–	32:1 MUX 2-tap FFE 28GHz PLL
RX function	CTLE 1-tap DFE 4:16 DMX	CTLE CDR 1:8 DMX	CTLE 2-tap FFE 3-tap DFE	CTLE 1-tap DFE CDR 4:32 DMX Eye mon. adaptation

Summary

- The most power efficient 56.2-Gb/s/lane transceiver in 28-nm CMOS is presented
- Power efficiency is 4.4mW/Gb/s
  - A baud-rate sampling with a new phase detection scheme
  - Look-ahead DFE selector
  - 1 comparator eye monitor
- CDR and eye monitor are implemented
- A 2-tap FFE, CTLE, and 1-tap DFE compensate for an 18.4-dB loss

A 45 Gb/s PAM-4 Transmitter Delivering 1.3Vppd Output Swing with 1V supply in 28nm CMOS FDSOI

M. Bassi[1], F. Radice[2],

M. Bruccoleri[2], S. Erba[3], A. Mazzanti[1]

[1] Università degli Studi di Pavia, Pavia, Italy

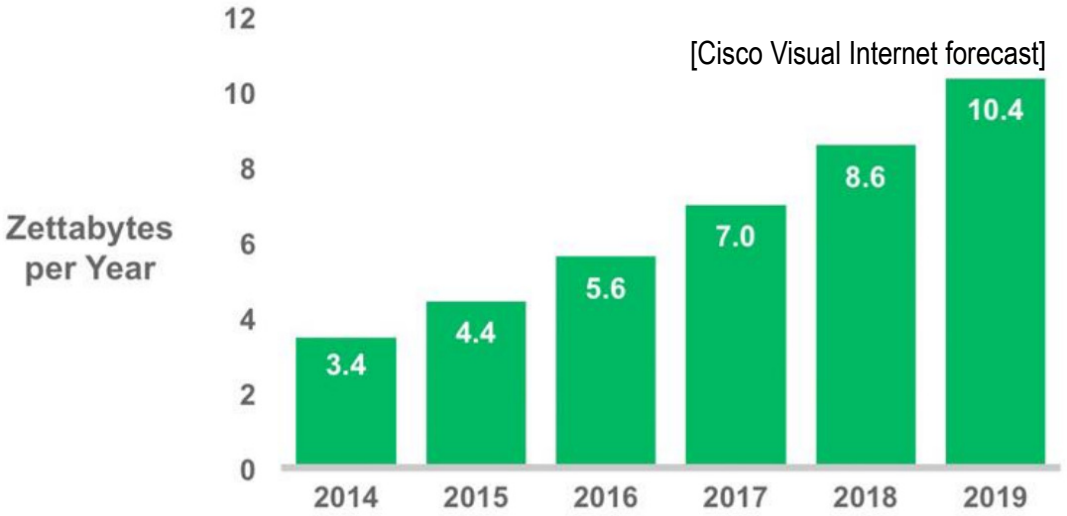
[2] STMicroelectronics, Cornaredo, Italy

[3] STMicroelectronics, Pavia, Italy

Outline

- **Motivation**
- **PAM-4 vs NRZ Signaling**
- **TX Architecture**
  - High-Swing Driver
  - High-Speed Serializer
- **Measurement Results**
- **Conclusions**

Network Traffic Growth

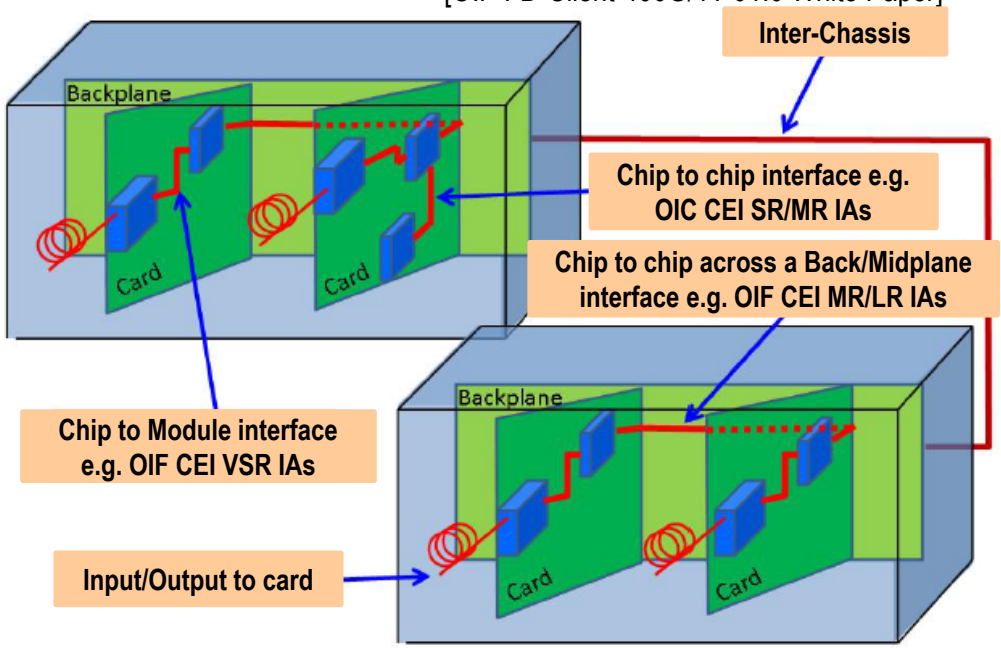


- 2.8x traffic growth from 2014 to 2019
- Up to 3.5x in busy-hour time
- Traffic from mobile devices will exceed that from wired devices by 2019

Answer to >25Gb/s interfaces:

- OIF CEI-56G LR/MR/VSR/XSR/USR roadmap
- IEEE 802.3bs 400GbE task force (16x25Gb/s or 8x50Gb/s)

[OIF-FD-Client-400G/1T-01.0 White Paper]



400G Challenges and Opportunities

Challenges

- Gate count increases faster than I/O speed
- Power dissipation, rather than technology and routing, mostly limits max I/O density
- Increasing data rate at > 25Gb/s increases link losses and power consumption

Possible solutions

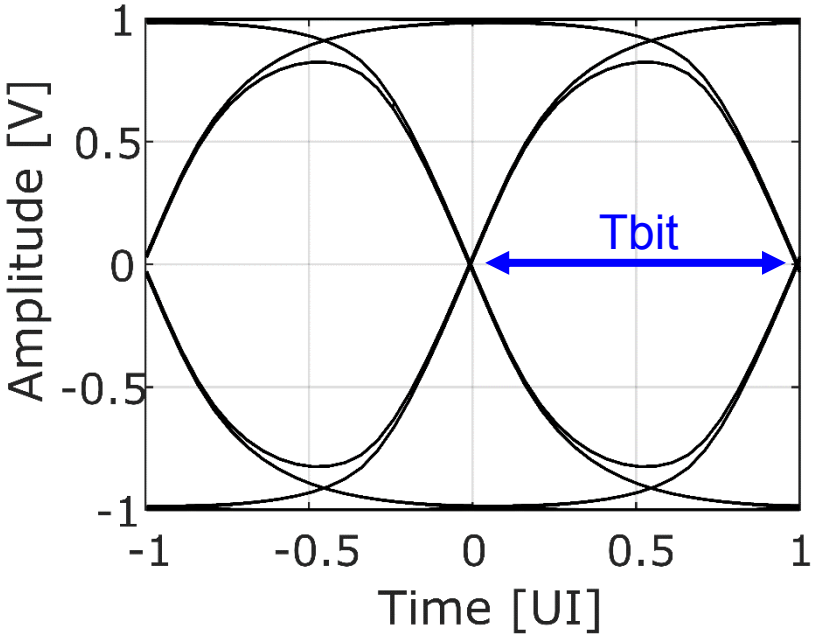
- Aggregate channels (WDM)
- Shorten electrical paths to optics
- Use complex modulation schemes

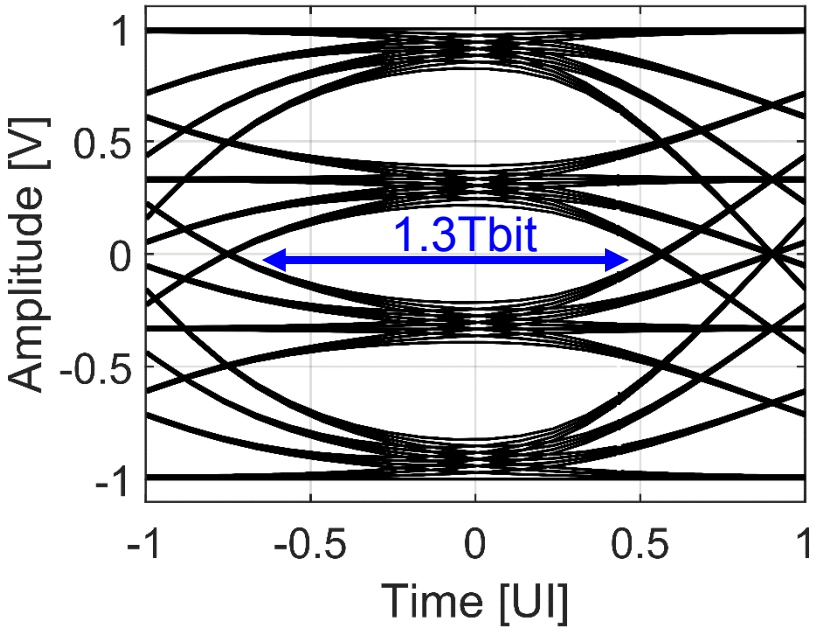
PAM-4 modulation

- Helps maintain loss budget by decreasing Nyquist frequency
- SNR degradation can be recovered by using FEC

PAM-4 SNR and H Opening

56Gb/s, ch. loss is 3dB @ 28GHz





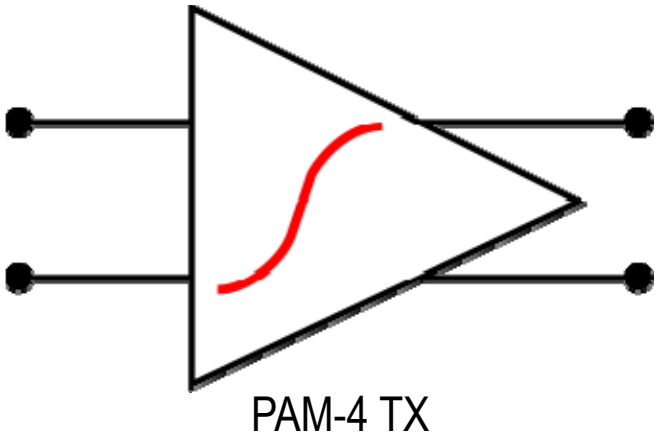
Intrinsic H opening = 1 [UI]
$f_{Nyquist}$ = 1/(2Tbit)
Eye Amplitude = 1

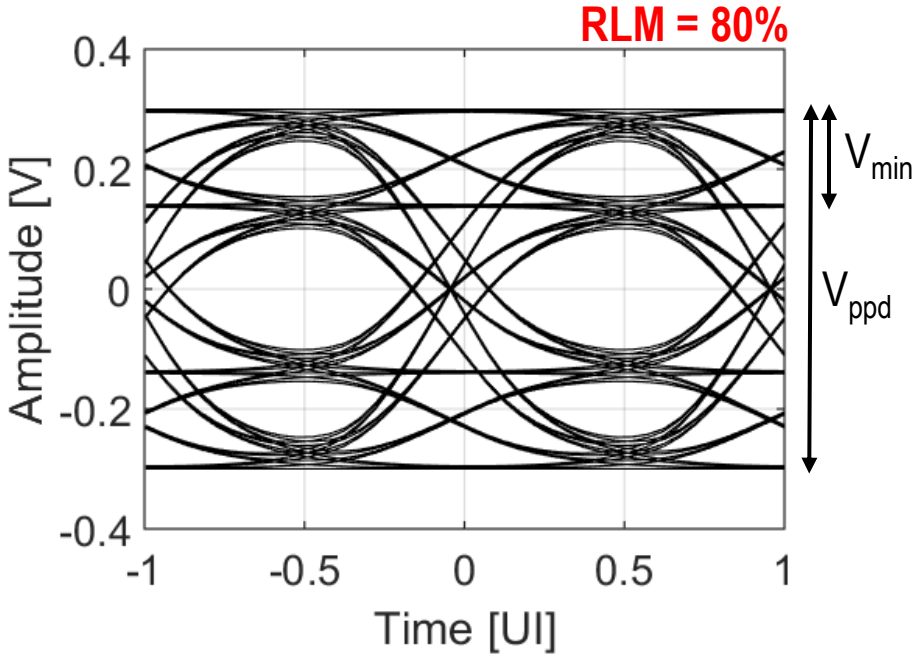
Intrinsic H opening = 1.3 [UI]
$f_{Nyquist}$ = 1/(4Tbit)
Eye Amplitude = 1/3

- Slight increase in horizontal opening
- Noise power is halved, but eye amplitude reduced by 1/3

Delivering high TX amplitude mandatory to preserve high SNR

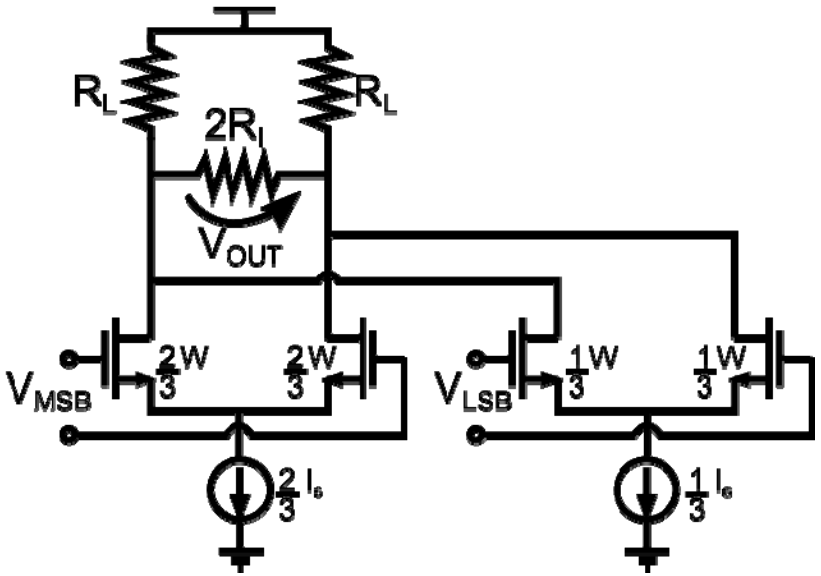
Eye Distortion due to TX Nonlinearity

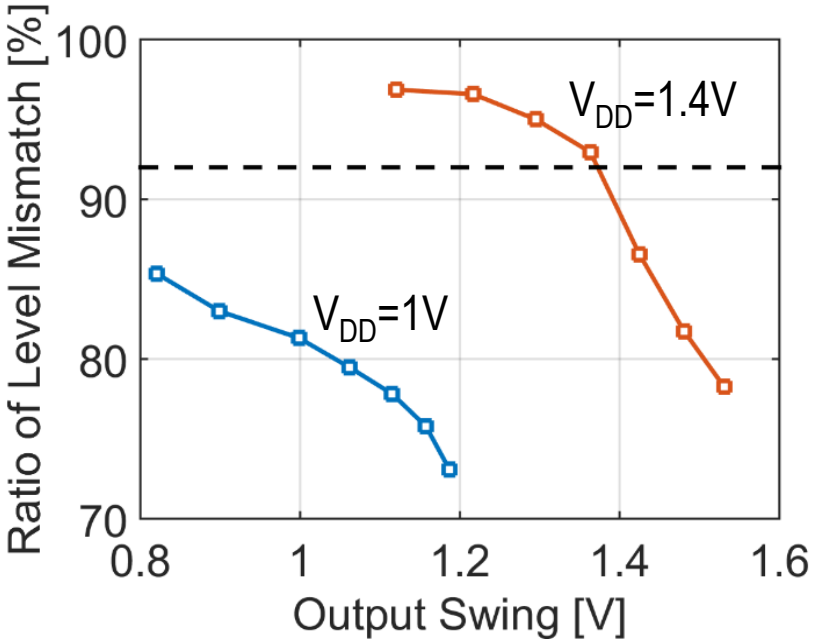




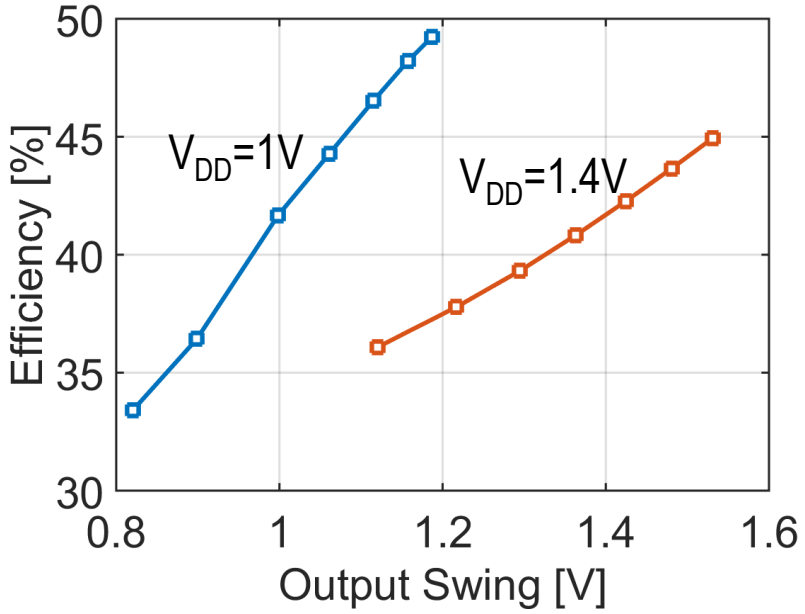
- Ratio of Level Mismatch (RLM) quantifies PAM-4 eye distortion
- RLM = $3V_{min}/V_{ppd}$ = 80% (picture above) yields:
  - 25% reduction in H opening → H opening advantage lost
  - 30% reduction in vertical opening @ 10E-6 with 3mVrms noise
- Standard recommends RLM>92%

Current-Mode Driver

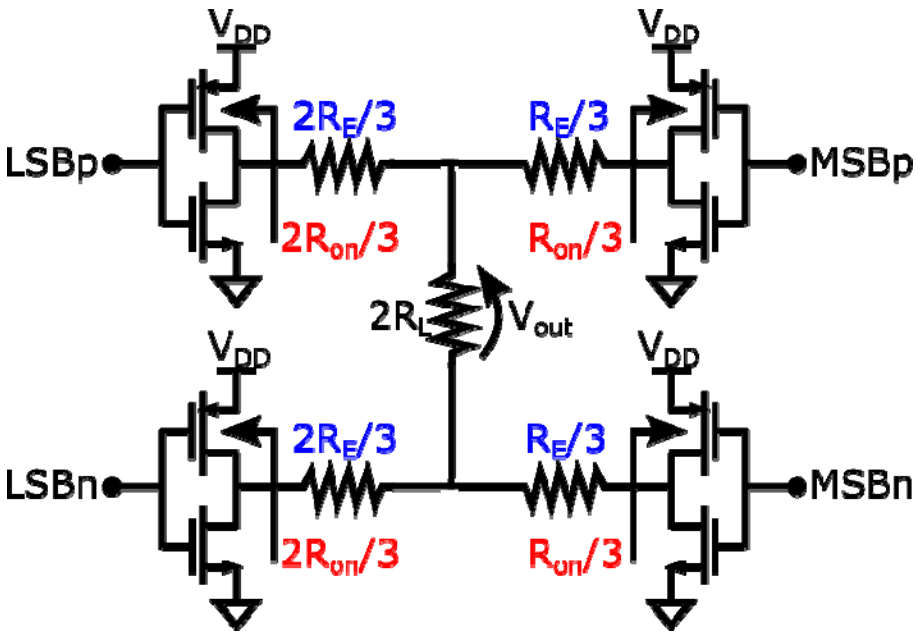


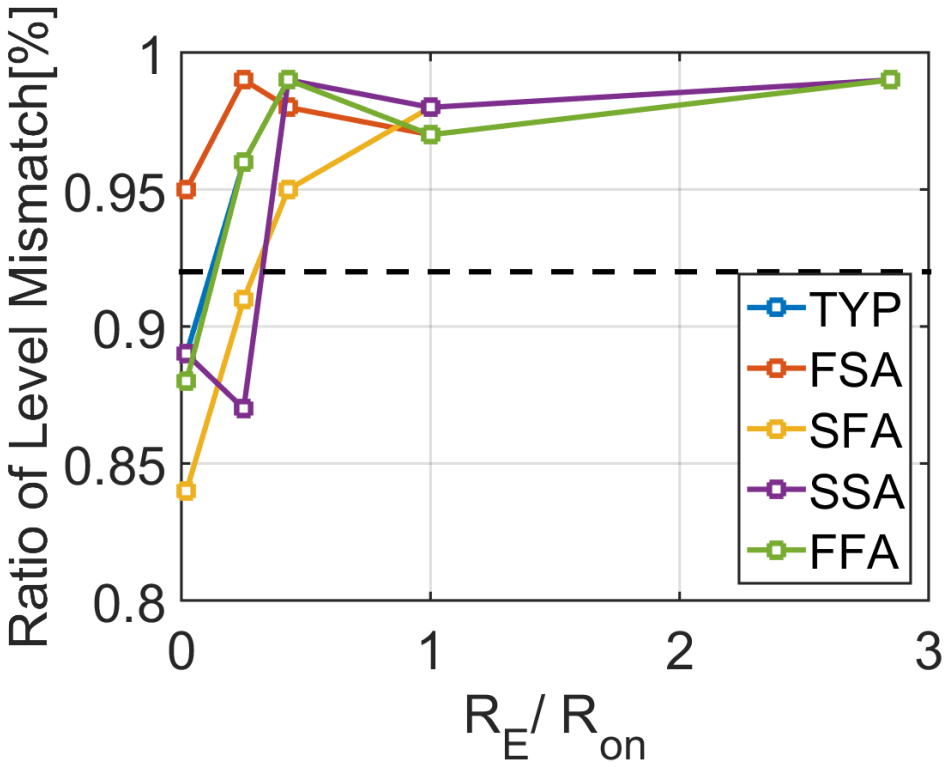


- Theoretical max diff. swing is $4/3(V_{DD}-V_{OV})$
- Linearity limited by tail current sources
- With V_{DD}=1V, typically RLM<85%
- Increasing V_{DD} increases linearity but reduces efficiency



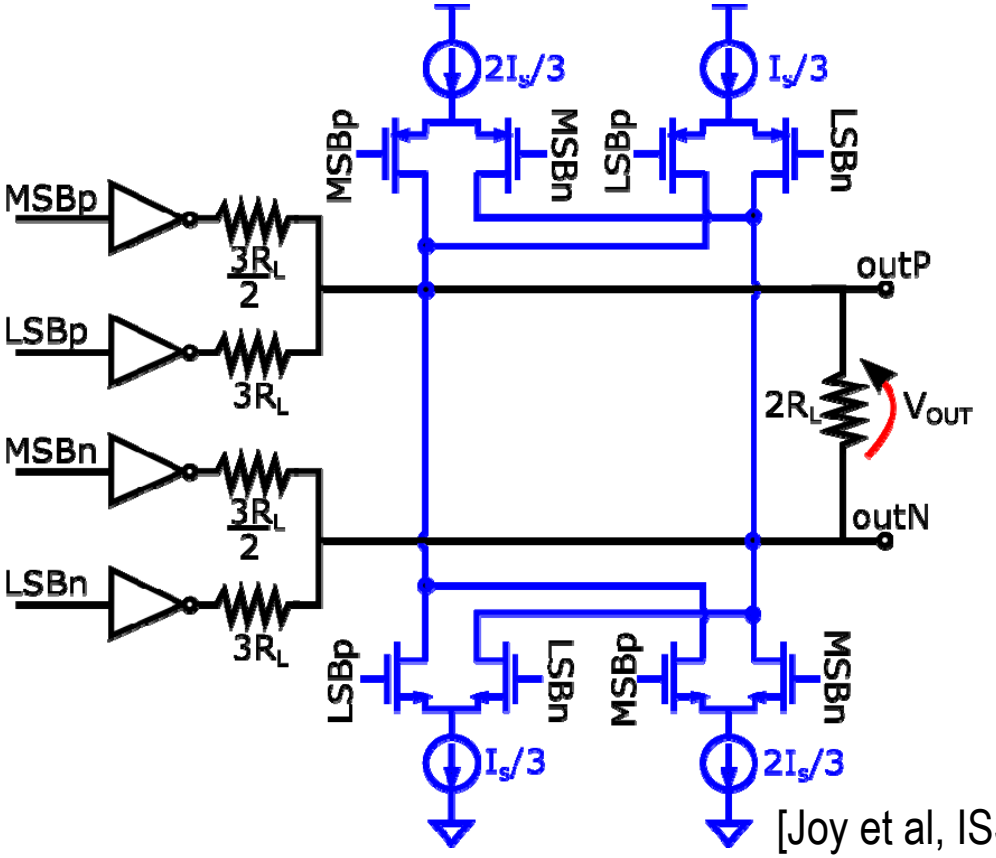
Voltage-Mode Drivers

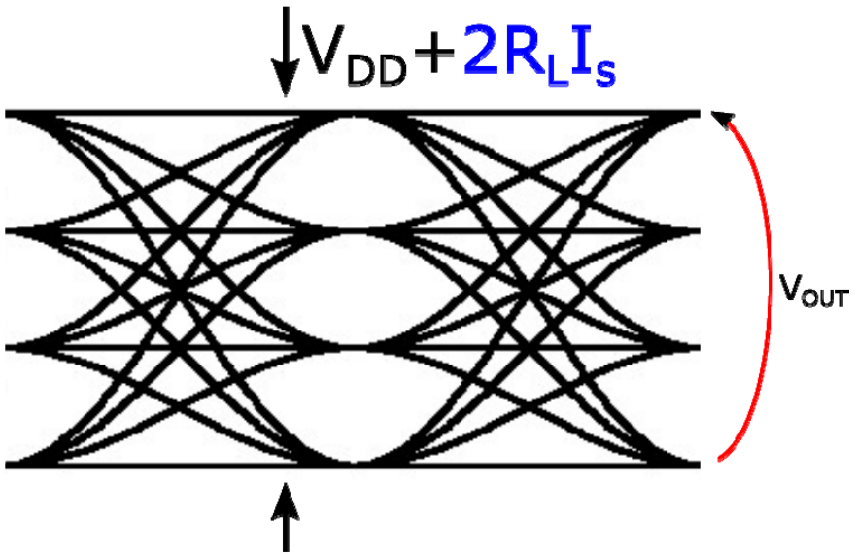




- Robust towards non-linear device on-resistance R_T
- With R_E/R_{on}>1/1, RLM is better than 96%
- However, matching constrains max swing to V_{DD}

Proposed Swing-Enhanced PAM-4 TX

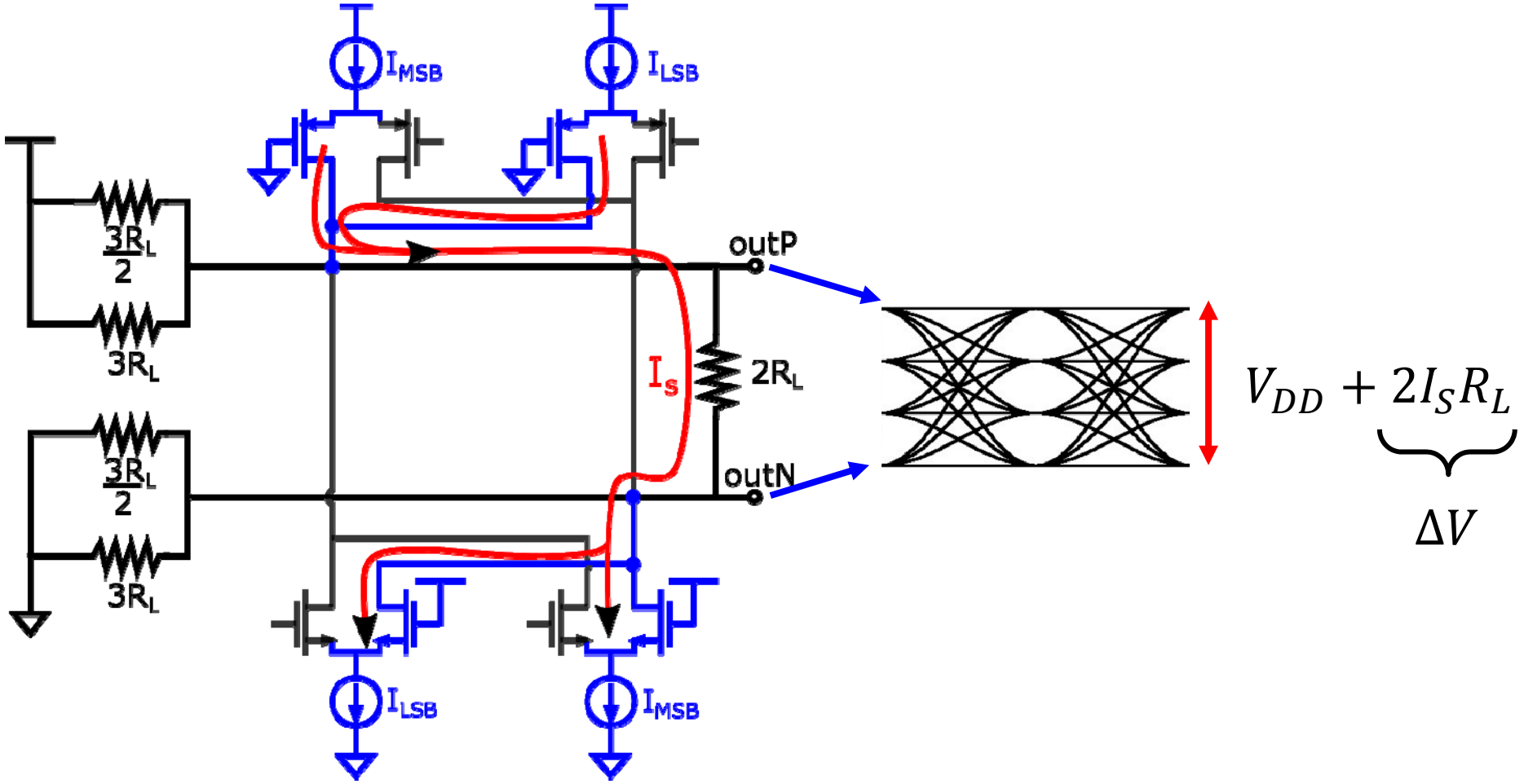




[Joy et al, ISSCC '11]

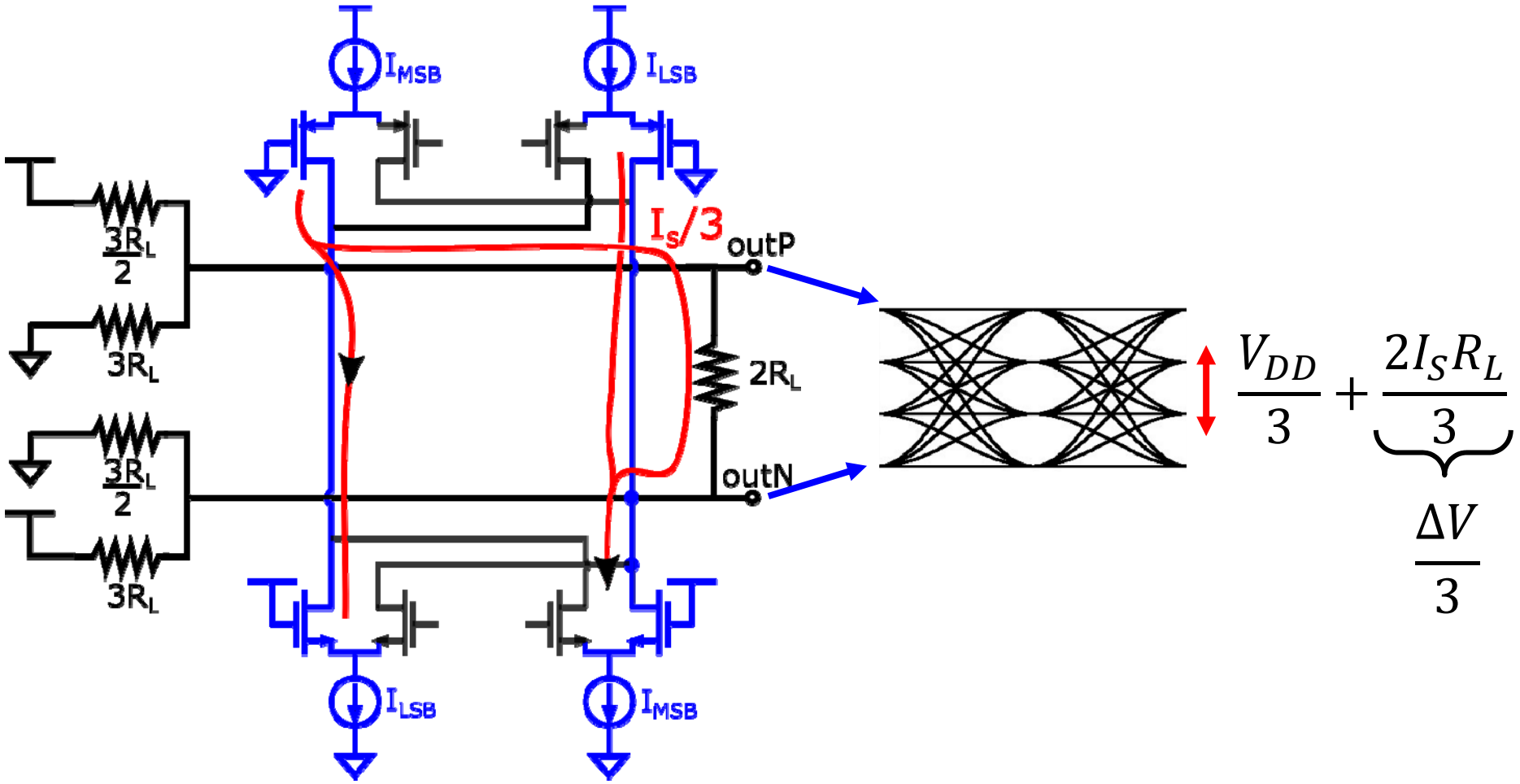
- Additional currents ($1/3I_s$,$2/3I_s$) injected in the output node
- With I_s=3mA, V_{DD}=1V, output swing is raised to 1.3Vppd
- Compared to increasing V_{DD} to 1.3V, 30% better efficiency

Proposed Swing-Enhanced PAM-4 TX



- Driver is transmitting MSB=1 and LSB=1
- Additional current flowing into the load is $I_S = I_{MSB} + I_{LSB}$

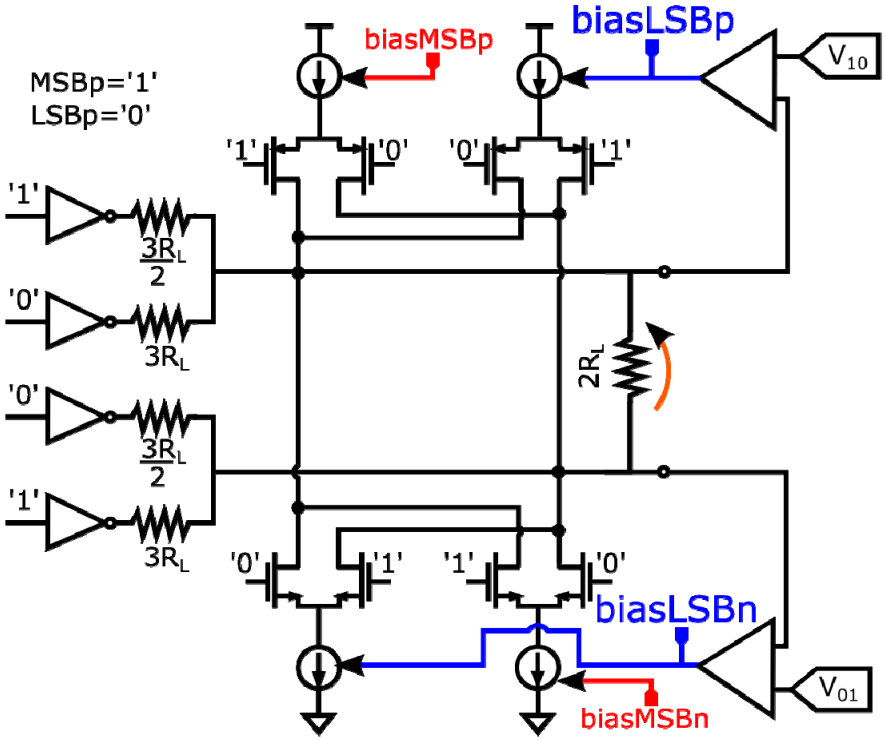
Proposed Swing-Enhanced PAM-4 TX

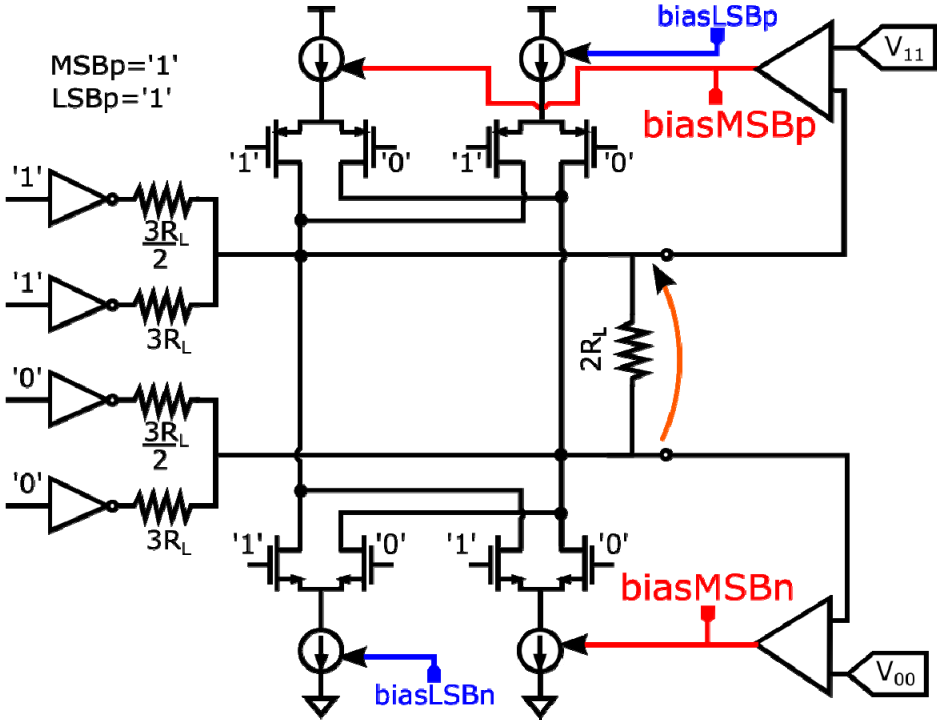


- Driver is transmitting MSB=1 and LSB=0
- Additional current flowing into the load is $I_S/3 = I_{MSB} - I_{LSB}$

TX Replica Bias for Levels Calibration

- Small headroom across current sources when delivering large swing ⟶ linearity impaired and eye still distorted
- Scaled TX replicas employed for calibration of current sources

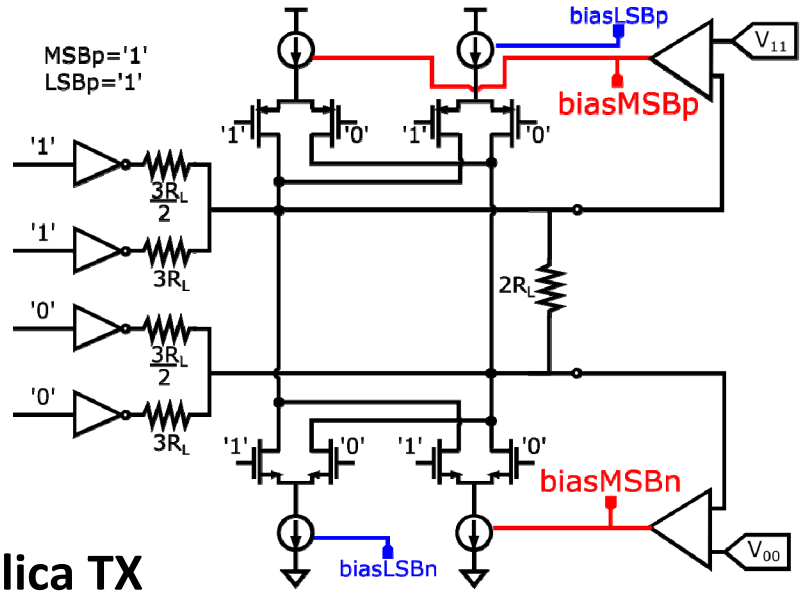


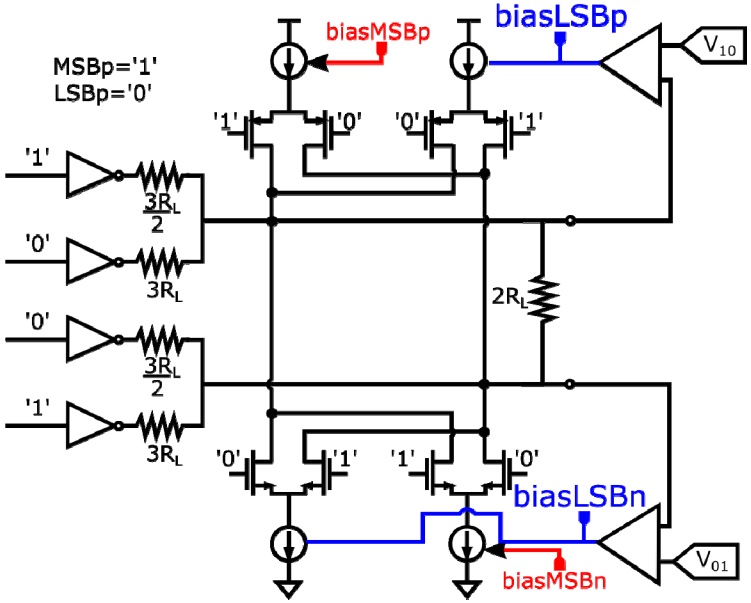


$$I_{MSB} - I_{LSB} = \frac{\Delta V}{6R_L}$$

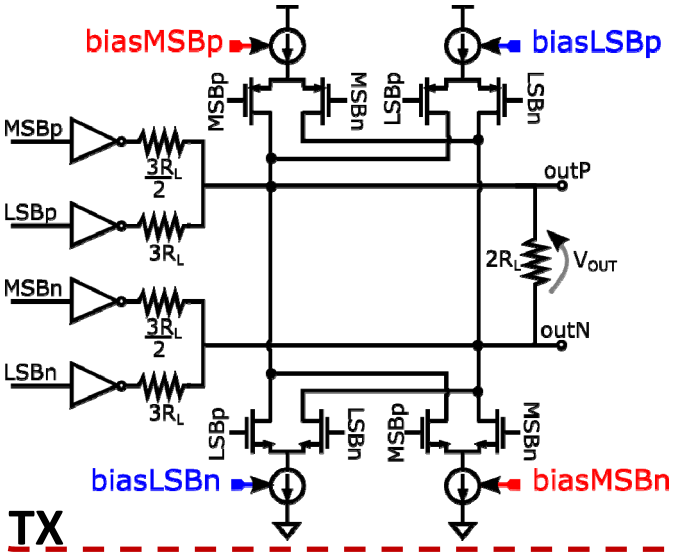
$$\alpha(I_{MSB} + I_{LSB}) = \frac{\Delta V}{2R_L}, \alpha < 1$$

TX Replica Bias for Levels Calibration





Replica TX

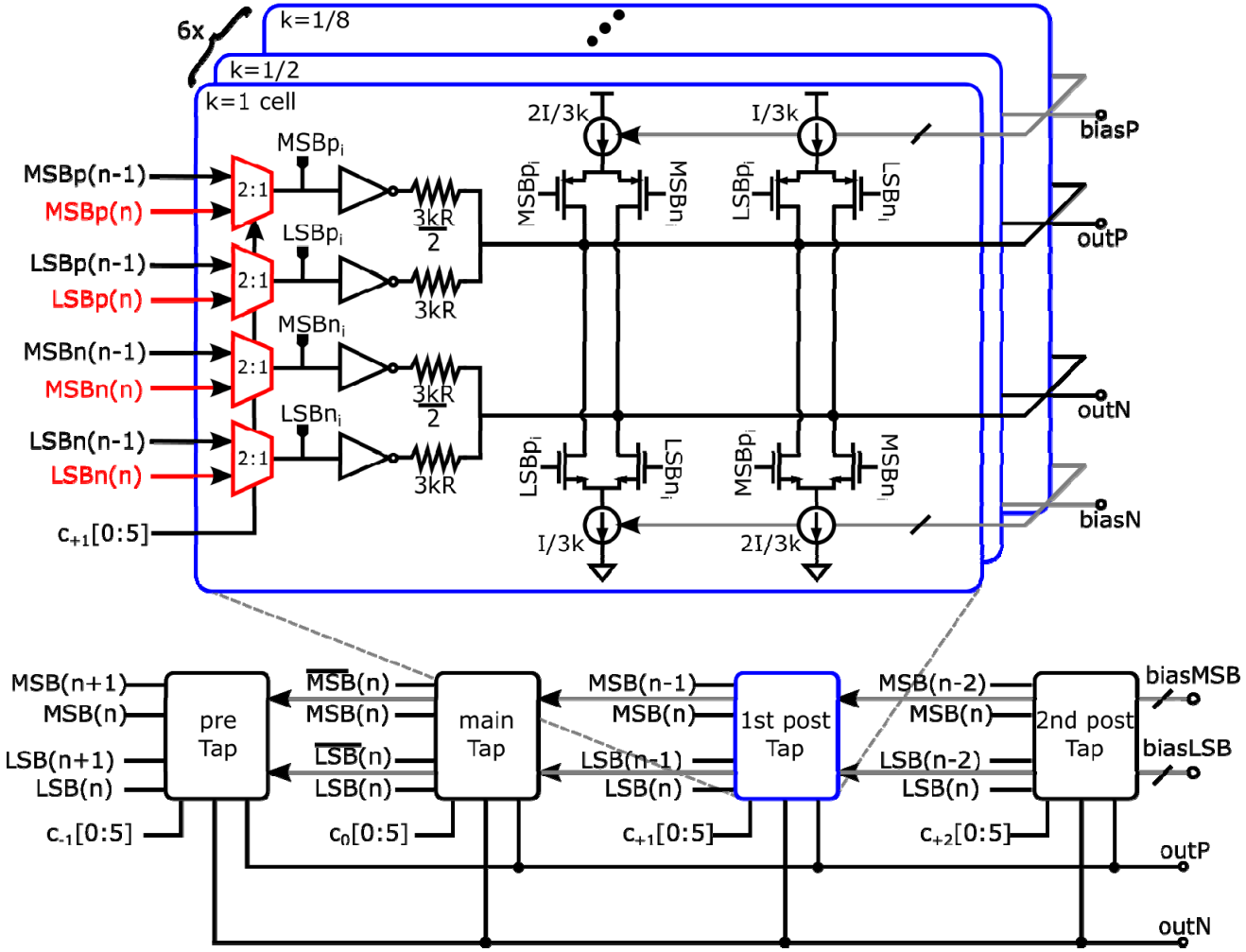


TX

Ensures high linearity even with small headroom across current sources:

- Without cal: RLM=83%
- With cal: RLM=97%

TX Driver with FFE



- Multiplexers switch either main tap stream or delayed data to the driver
- Each tap made of 6 slices to implement FFE coefficients

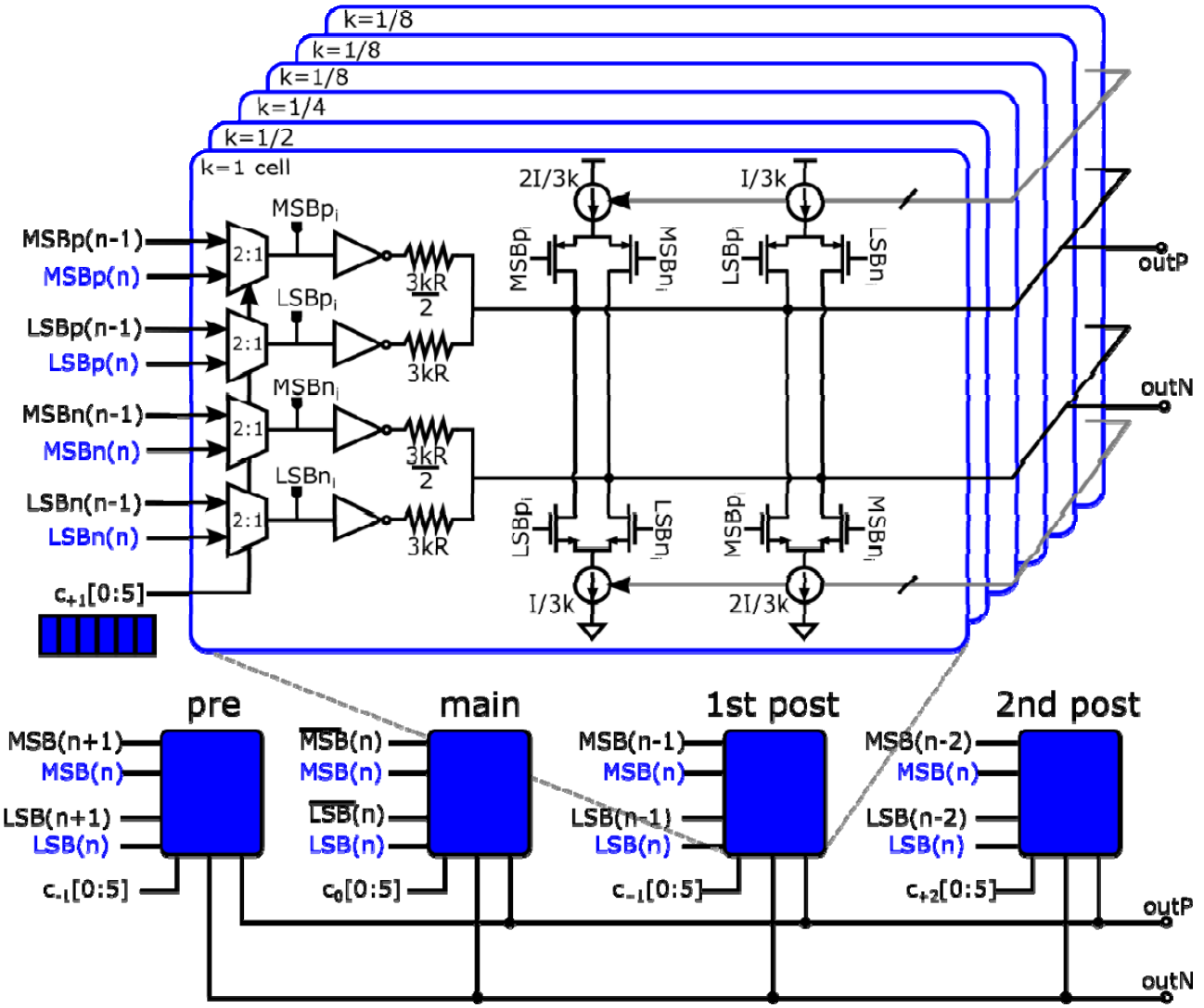
TX Driver with FFE

Coeff. Setting

Pre	31
Main	31
1° post	31
2° post	31

Coeff. Gain

C_{-1}	0
C_0	1
C_{+1}	0
C_{+2}	0



- All slices transmit the main data stream

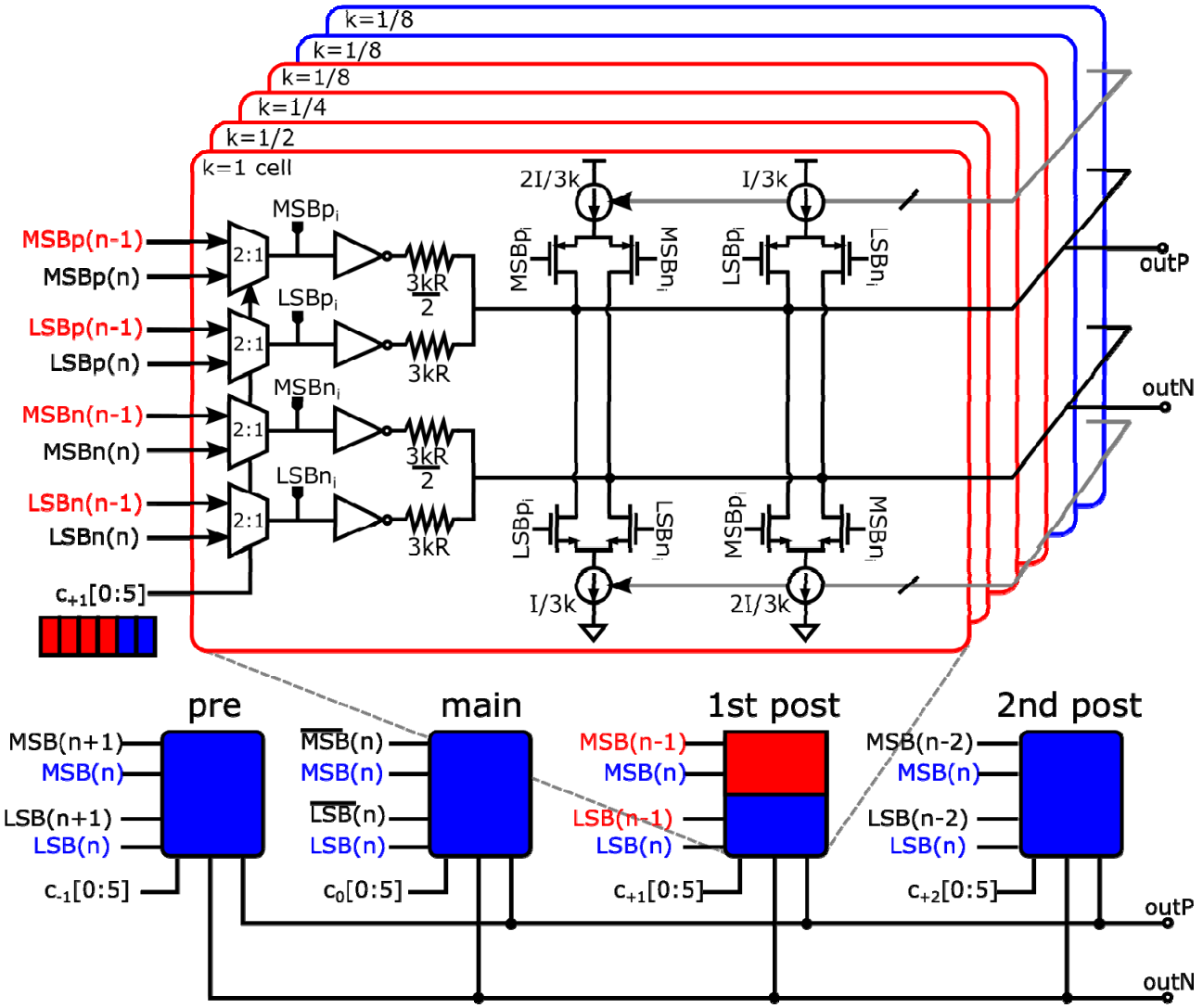
TX Driver with FFE

Coeff. Setting

Pre	31
Main	31
1° post	16
2° post	31

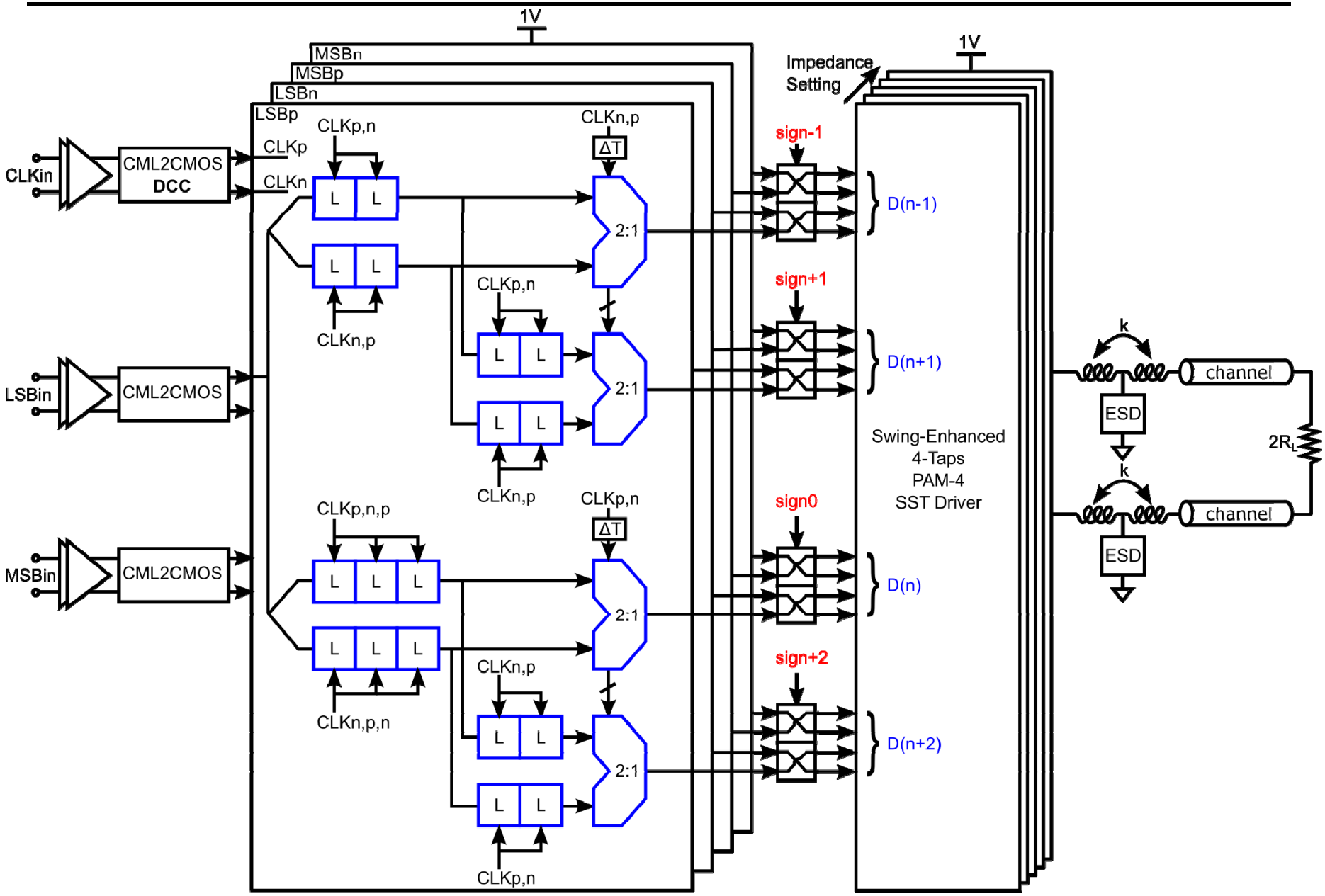
Coeff. Gain

C_{-1}	0
C_0	7/8
C_{+1}	1/8
C_{+2}	0

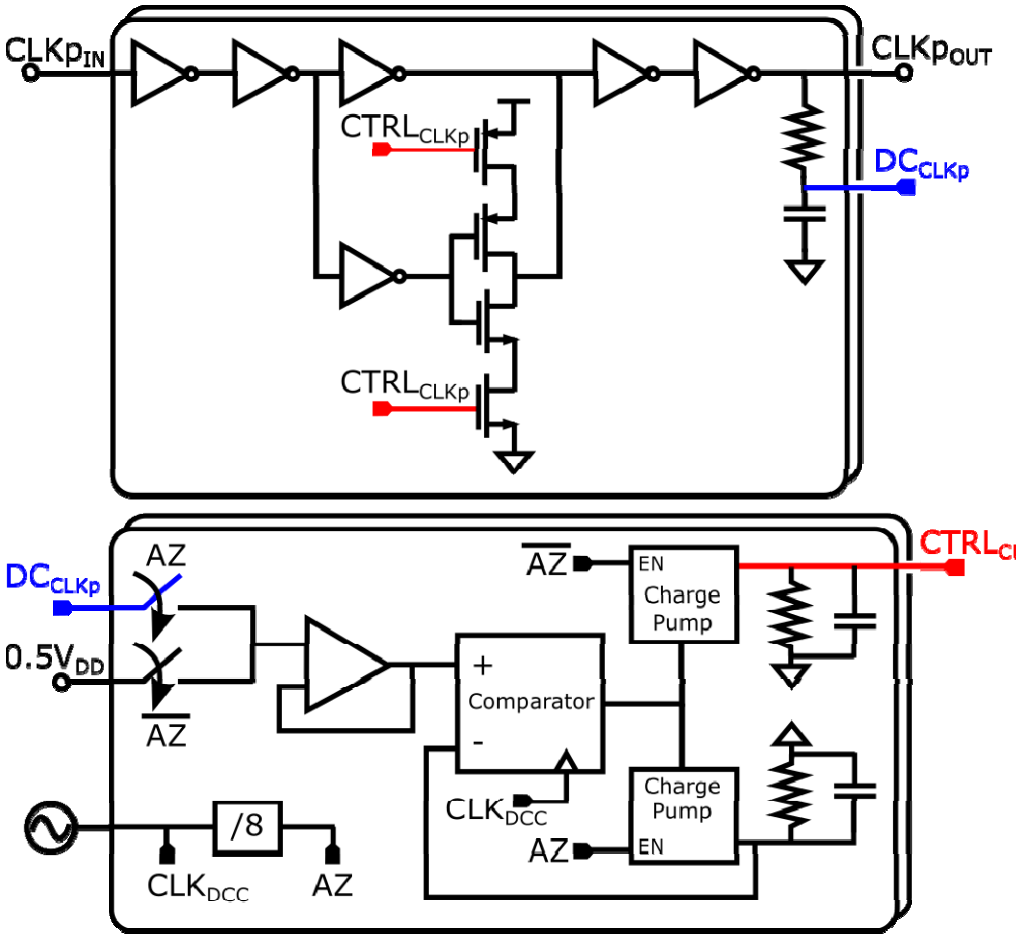


- Main tap gain always automatically maximized

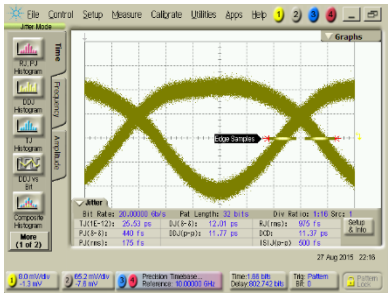
Serializer, Driver and Output Network



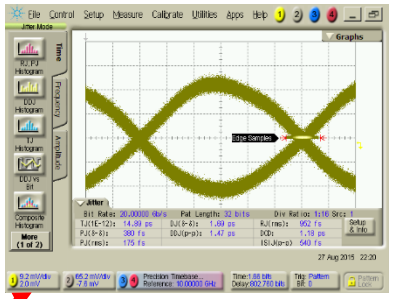
Duty Cycle Correction Circuit

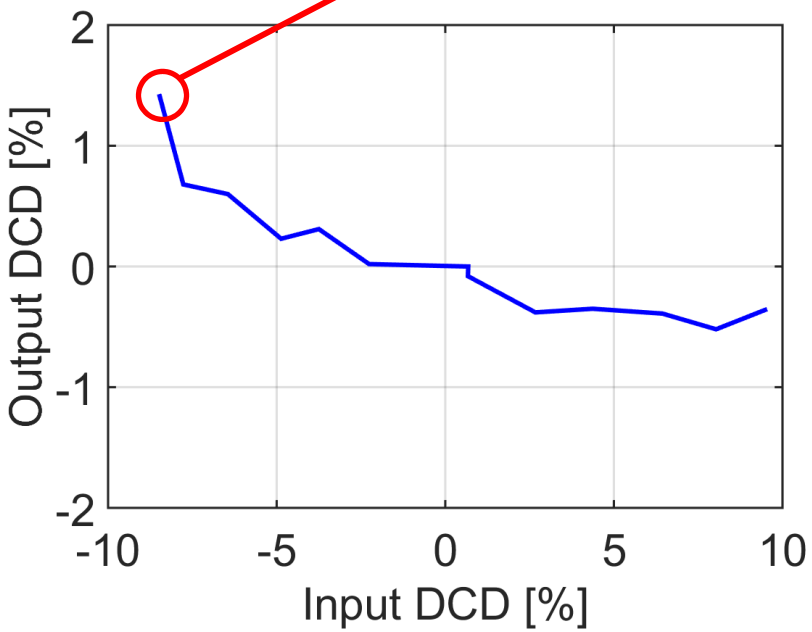


DCC Off



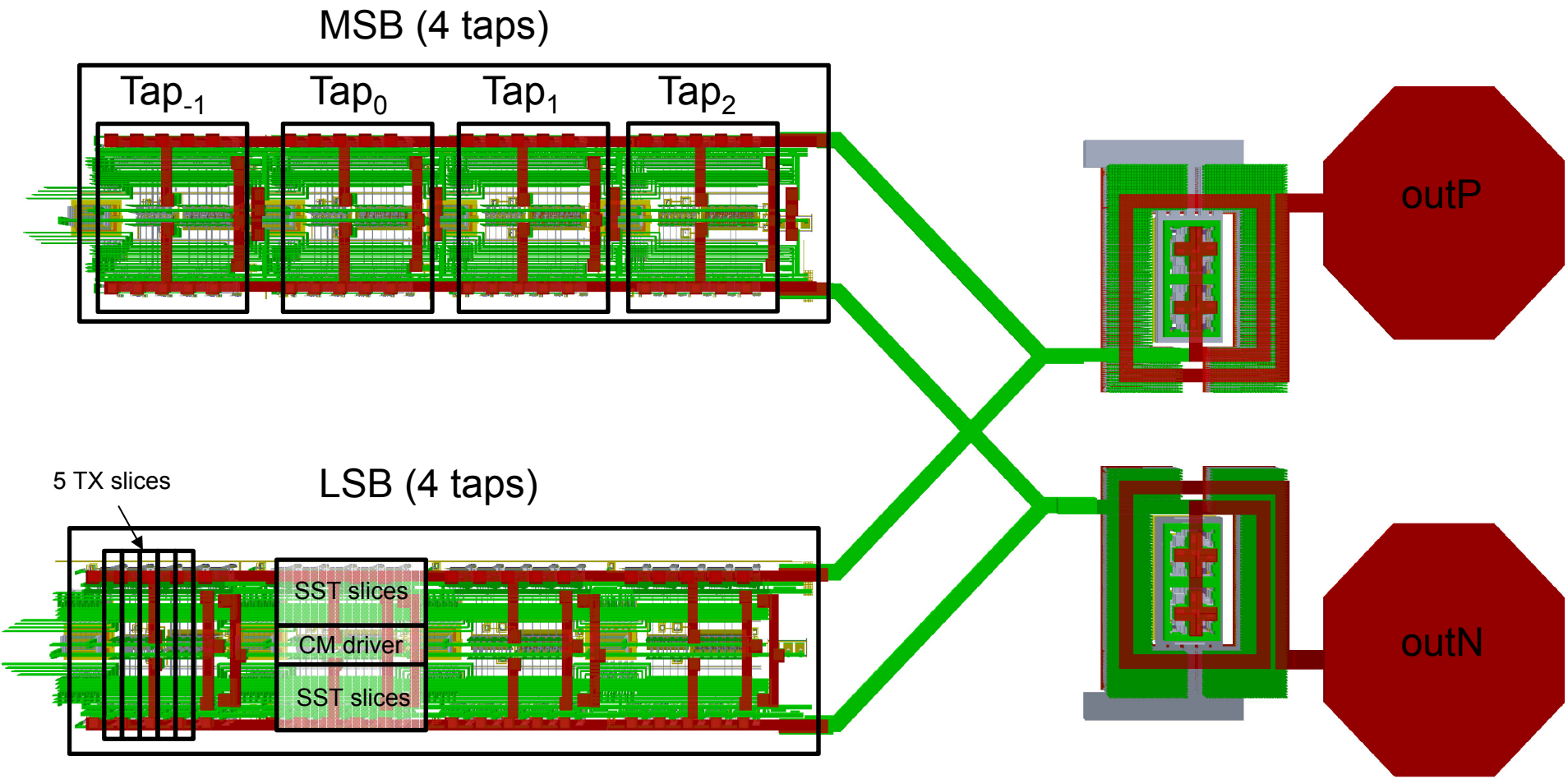
DCC On



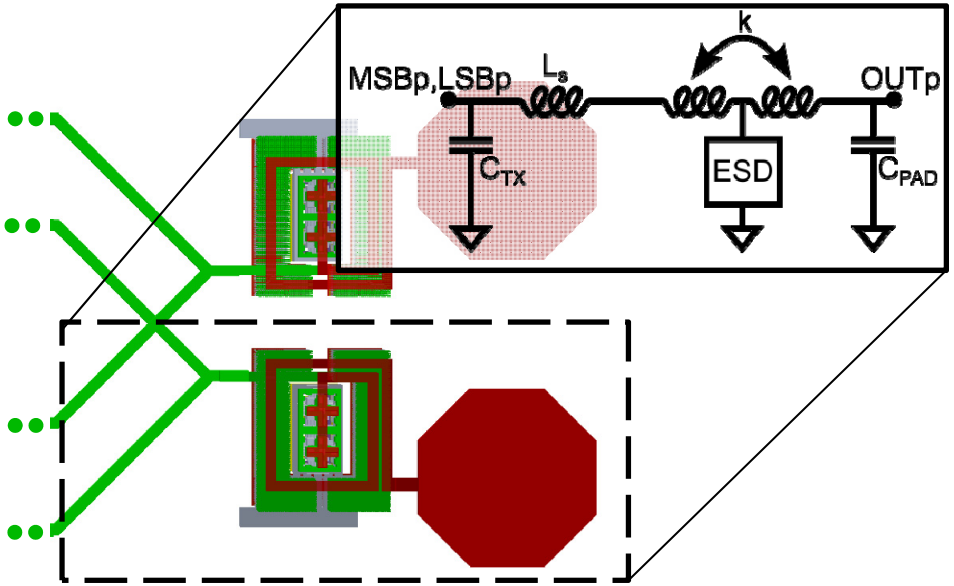


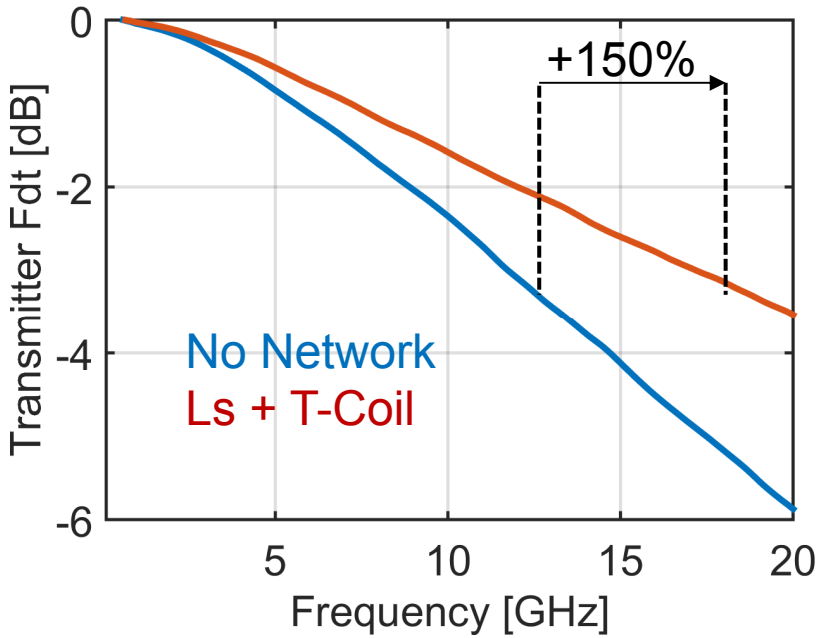
- DCC circuit recovers up to 9% input duty cycle distortion

Driver and Output Network Floorplan



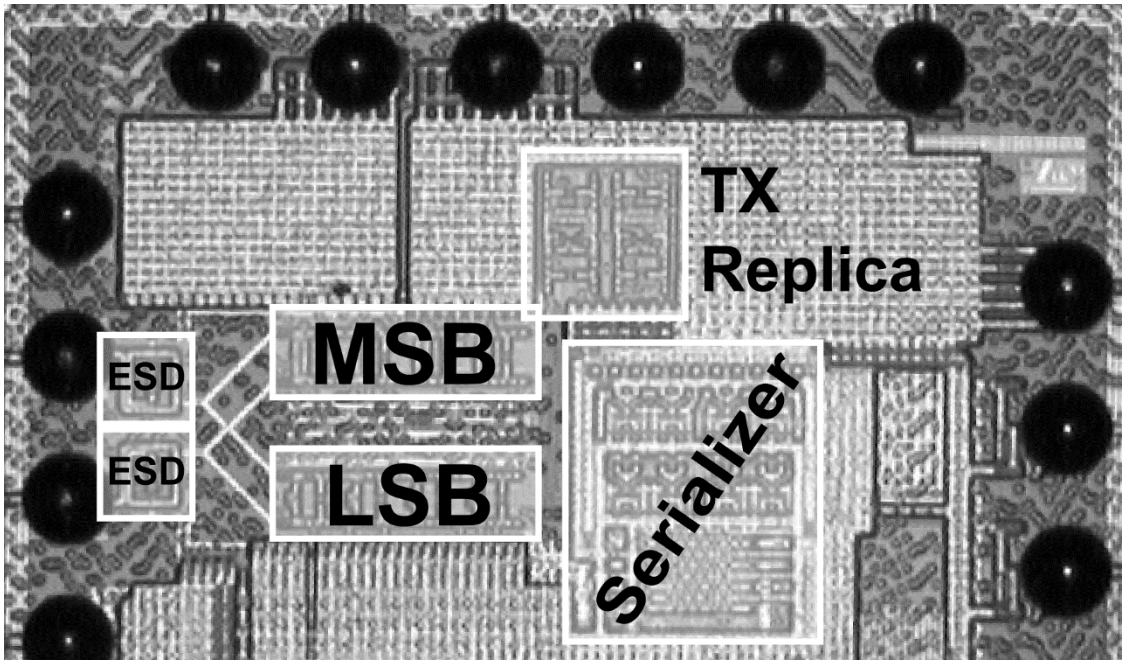
Output Network and ESD Protection





- 200V MM / 500V CDM, >>2kV HBM ESDs account for 250fF capacitance each
- Routing inductor L_s + asymmetric T-coil enhance bandwidth by 150%

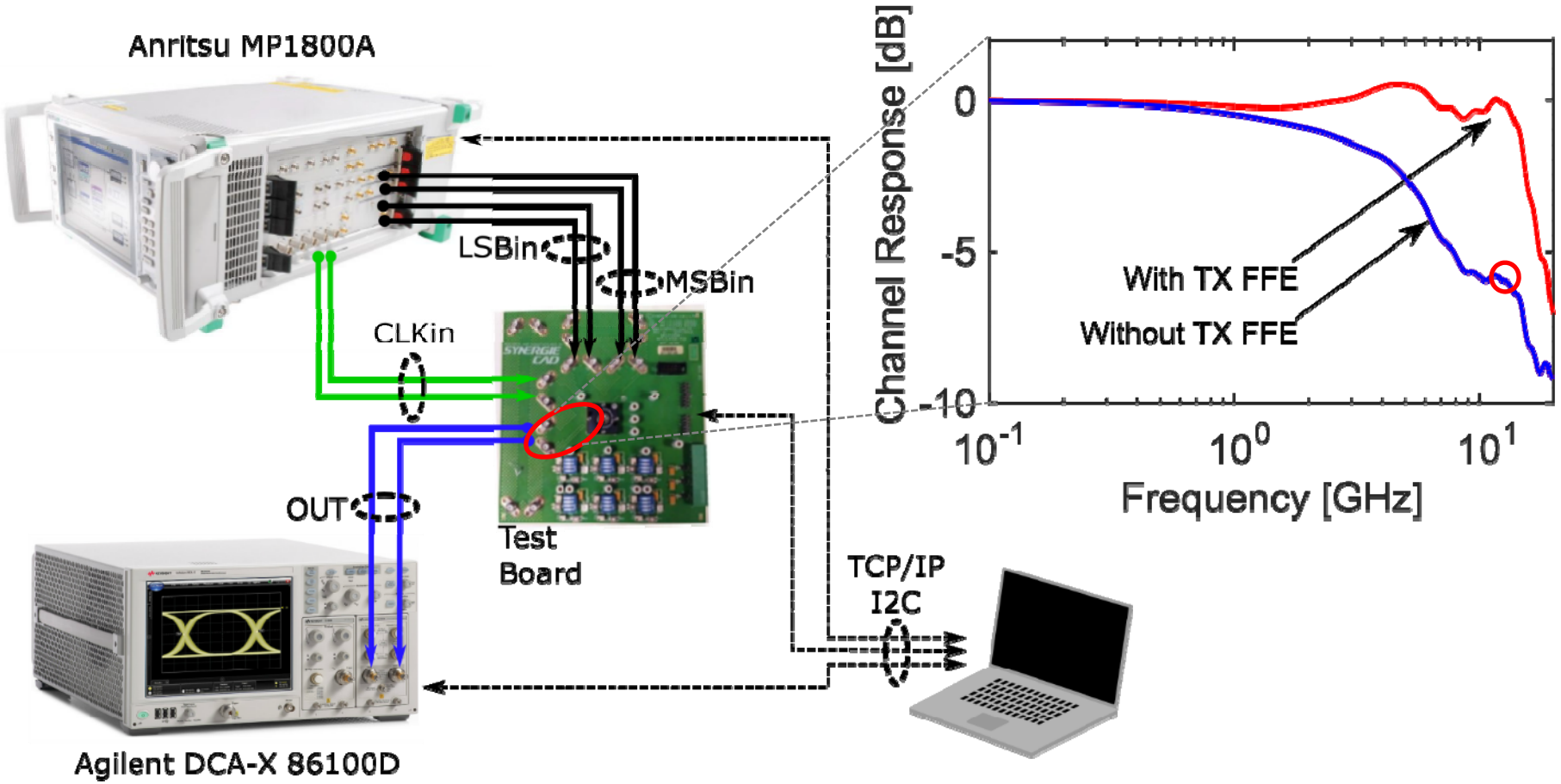
Test Chip



- Supply Voltage:1V
- Data Rate: 45Gb/s
- Power: 120mW
  - Serializer 60mW
  - Replica TX 5mW
  - Bias 5mW
  - Driver 50mW

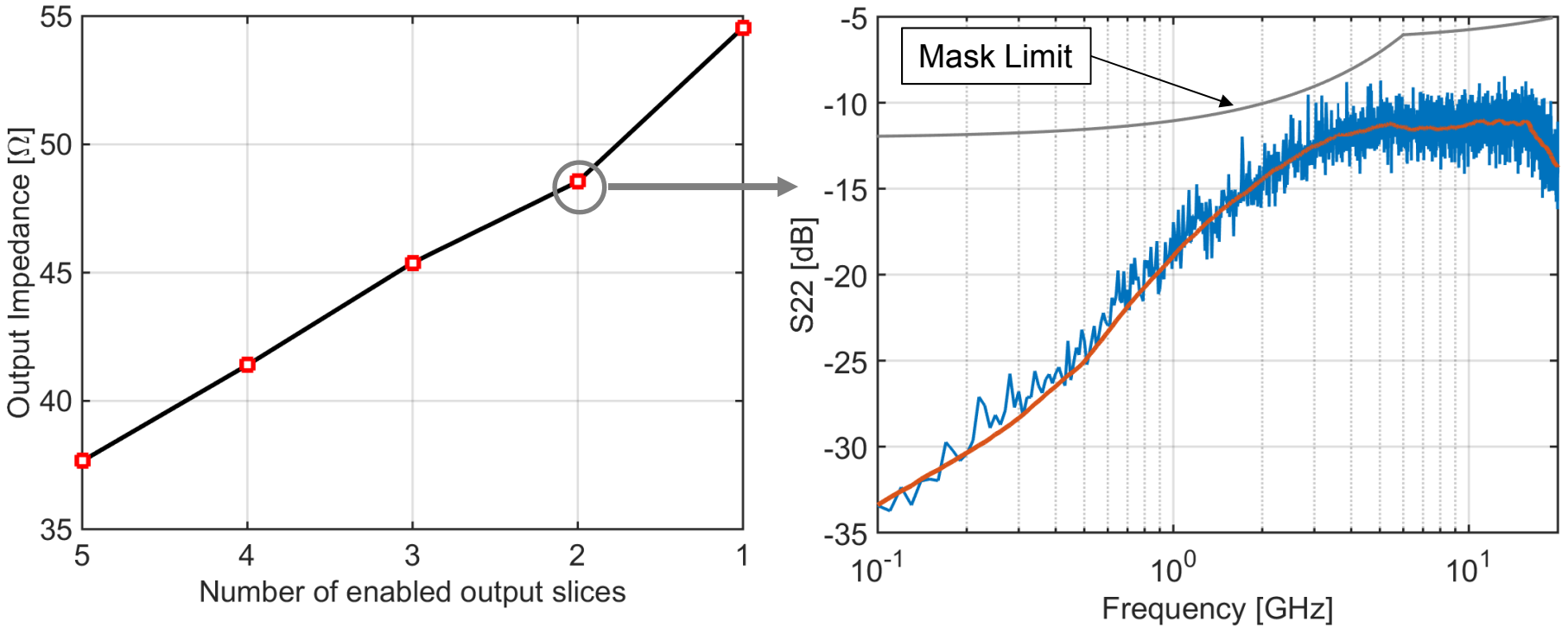
- 10ML CMOS 28nm FDSOI from STMicroelectronics
- Chips encapsulated in flip-chip BGA packages

Measurement Setup



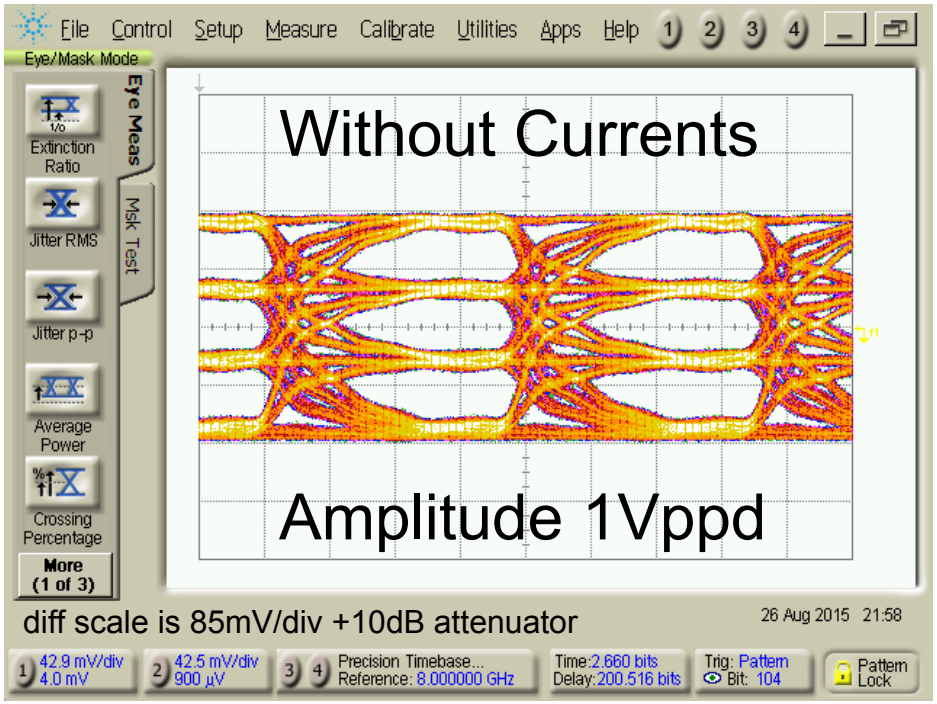
- Channel profile includes PCB trace, connector and cable losses
- At the frequency of 12GHz, loss is 6dB

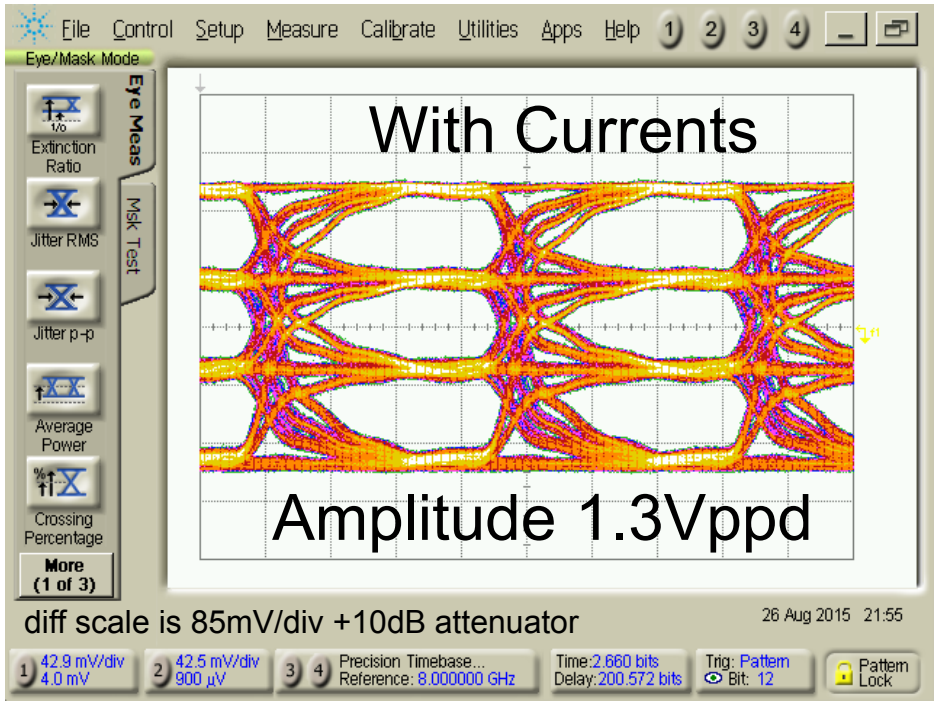
Differential Output Impedance



- Output impedance can be set with 4Ω precision
- Output return loss inside IEEE802.3bs mask limit

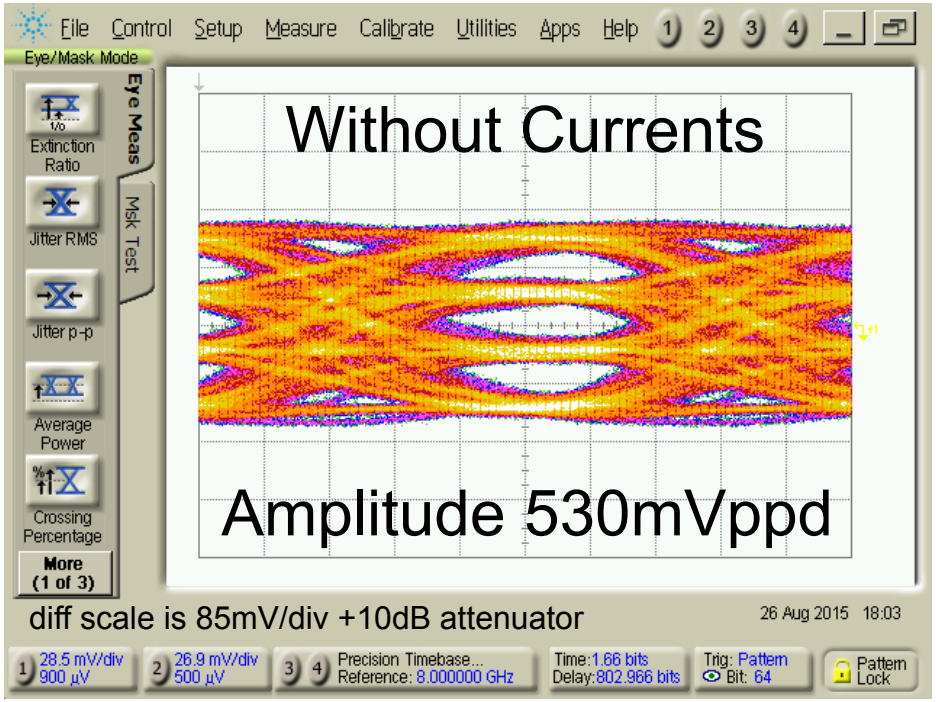
Output Eyes at 10Gb/s

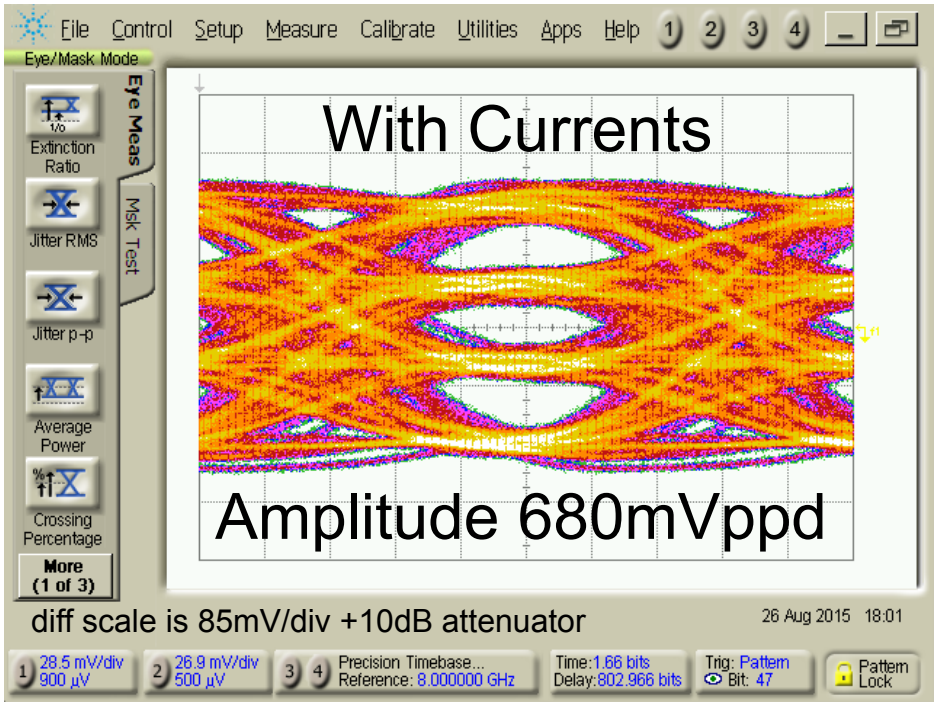




- Data Rate is 10Gb/s
- FFE disabled
- Swing-enhancing currents improve eye amplitude by 30%
- Output levels calibration loop set (V11, V10, V01, V00) ~ (825mV, 610mV, 390mV, 175mV)

Output Eyes at 45Gb/s

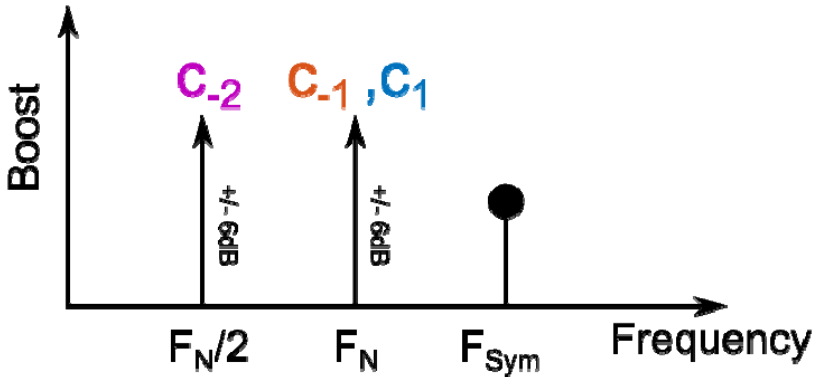


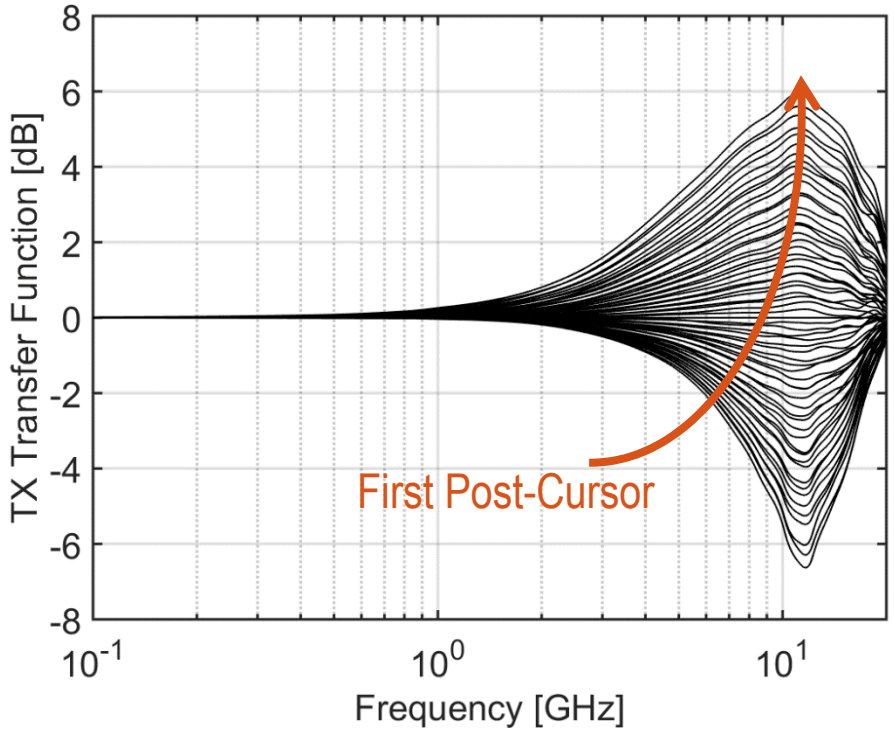


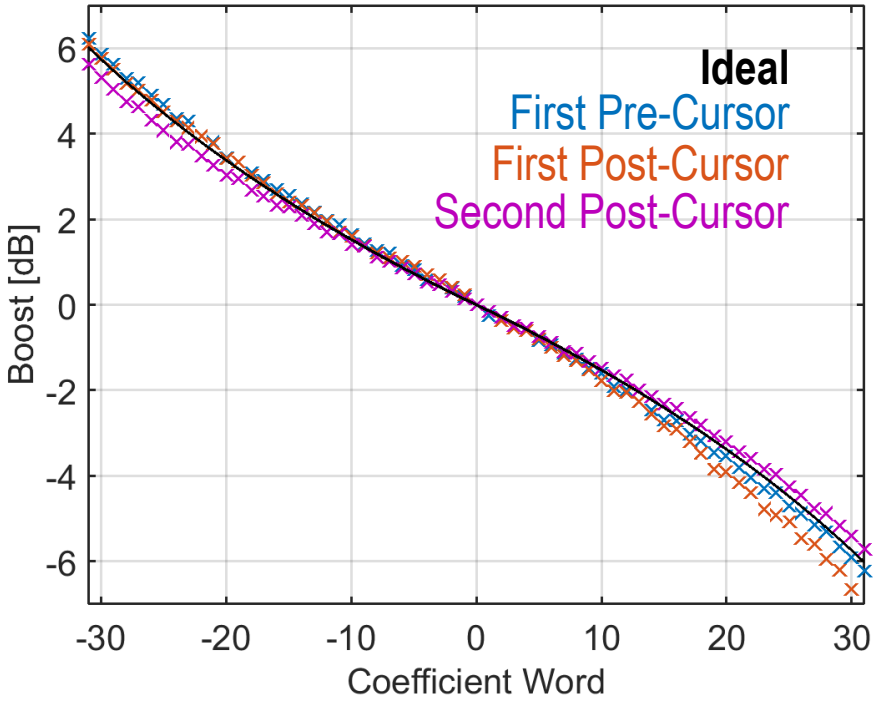
- Data Rate is 45Gb/s
- FFE is ON and recovers 6dB at Nyquist
- Swing-enhancing currents improve eye amplitude by 28%
- Output levels calibration loop set (V11, V10, V01, V00) ~ (825mV, 610mV, 390mV, 175mV)

Boost vs Coefficients

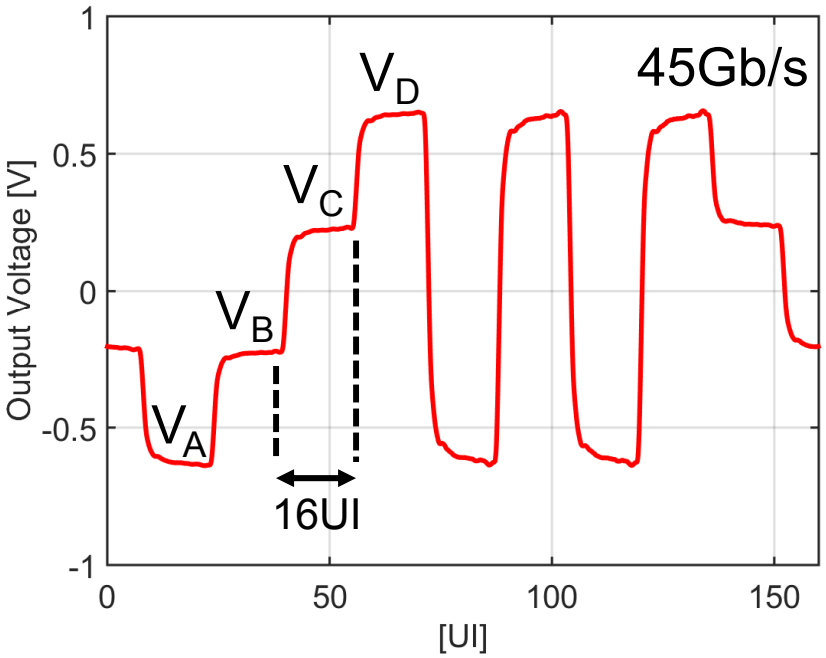
- Each coefficient provides maximum +/- 6dB boost
- Precision: 5 bits + sign

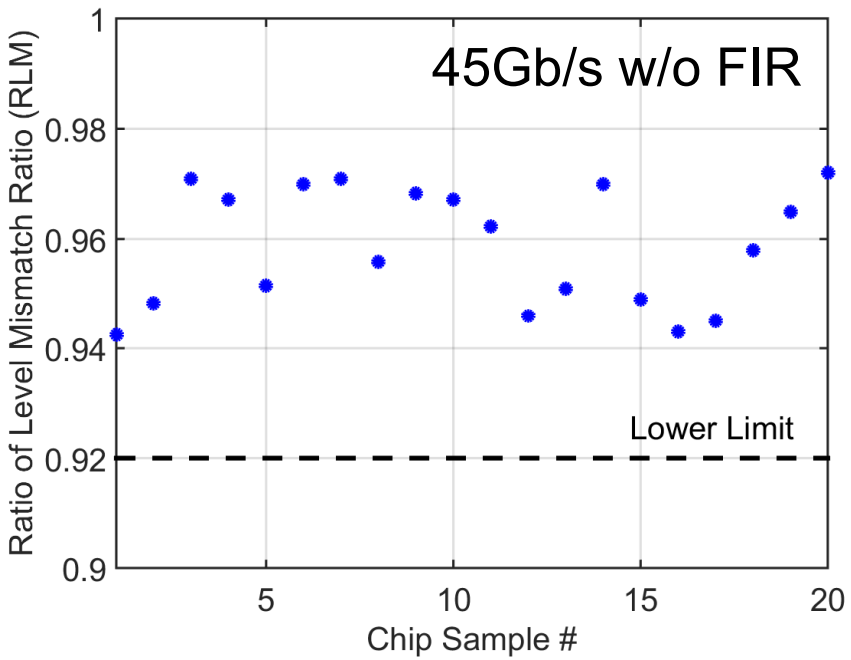






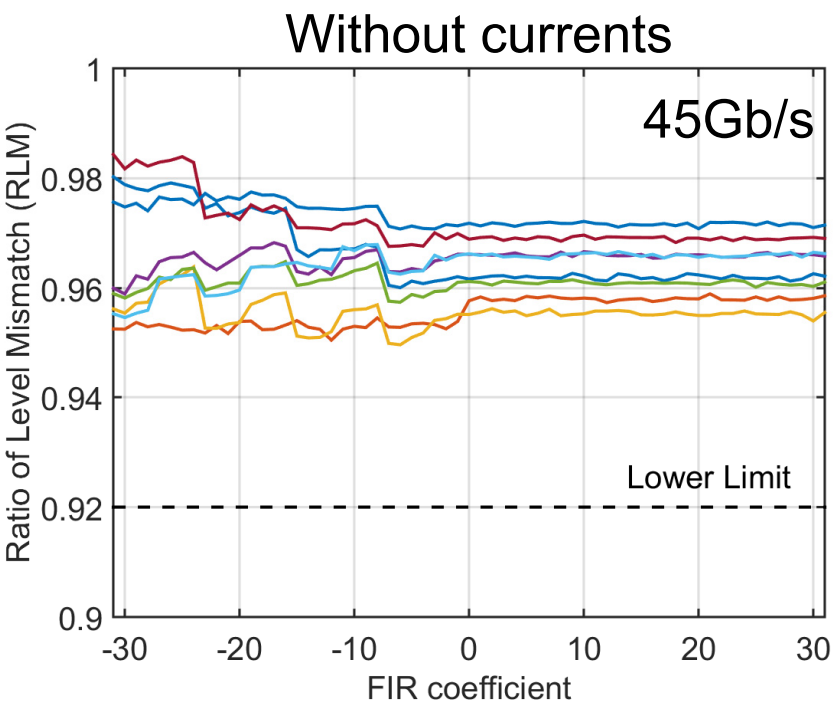
Eye distortion test 1/2

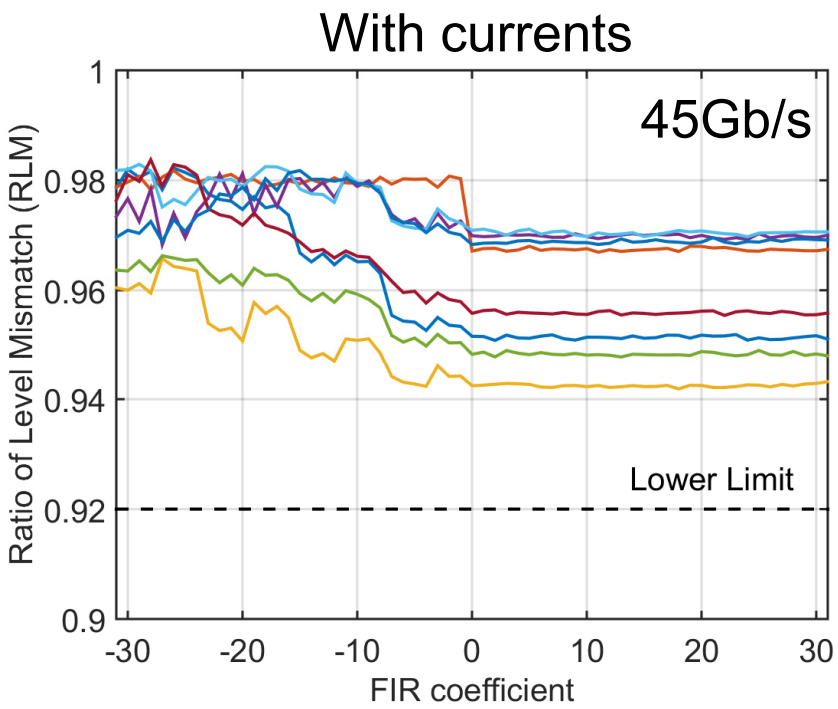




- Test proposed by CEI-56G and IEEE 802.3bs emerging standards
- RLM = 3 min(V_B-V_A,V_C-V_D,V_D-V_C)/(V_D-V_A)
- At 45Gb/s RLM > 0.92 (spec under discussion) for 20 chip samples

Eye distortion test 2/2





- RLM evaluated for 20 chip samples as a function of first post-cursor coefficient
- Equalization by using FFE does not impact RLM

Summary and comparison

Ref.	Menolfi ISSCC '05	Nazemi ISSCC '15	Chiang ISSCC '14	Kim ISSCC '15	This Work
CMOS Technology	90nm SOI	28nm	65nm	14nm	**28 nm FDSOI**
Driver Topology	CML	CML	CML	SST	**SST**
TX-FFE	4-taps	DAC	3-taps	No	**4-taps**
ESD	Yes	No	No	Yes	**Yes**
Data-Rate [Gb/s]	25	36	60	40	**45**
Output Swing Without FFE [Vppd]	0.84[1]	0.8	0.250	0.9[3]	**1.3**
Vdd [V]	1	1.5	1.2	N/A	**1**
Power P_{DC} [mW]	102	84[2]	205[2]	167.5[2]	**120**
Power Efficiency $(V_{out}^2/2R)/P_{DC}$ [%]	3.4	3.8	0.15	2.42	**7**
mw/Gbps	4	2.33	3.4	4.18	**2.6**
Area [mm^2]	0.052	0.05	1.14	0.0279	**0.28**

1 Amplitude from picture. Loss recovered by FFE de-embedded.

2 Not including PLL and clock distribution power.

3 Amplitude from picture. Loss recovered by software CTLE de-embedded.

Conclusions

- High TX pk-to-pk swing and low distortion are key features for high-speed PAM-4 transmitters
- A hybrid, mostly-SST, PAM-4 transmitter architecture is proposed to deliver 1.3Vppd output swing at 45Gb/s with 1V supply only
- Calibration through automatic loop ensures low eye distortion, a key requirement for next generation PAM-4 transceivers
- Measurements on more than 20 test chips realized in 28nm CMOS FDSOI technology prove the effectiveness of the proposed TX

A 40-to-64Gb/s NRZ Transmitter with Supply-Regulated Front-End in 16nm FinFET

Yohan Frans, Scott McLeod, Hiva Hedayati, Mohamed Elzeftawi, Jin Namkoong, Winson Lin, Jay Im, Parag Upadhyaya, Ken Chang

Xilinx, Inc., San Jose, CA

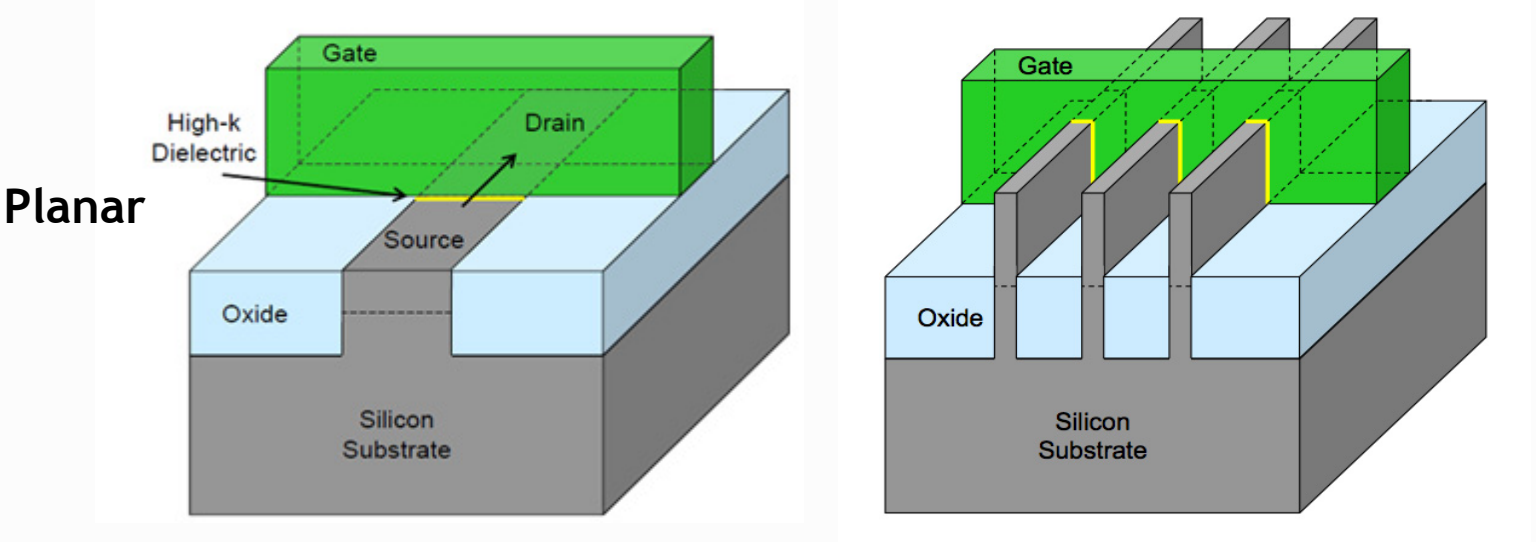
Outline

- Background
- Transmitter
  - Front-End
  - Clocking
- Phase Locked Loop
- Measurement Results
- Summary

Background

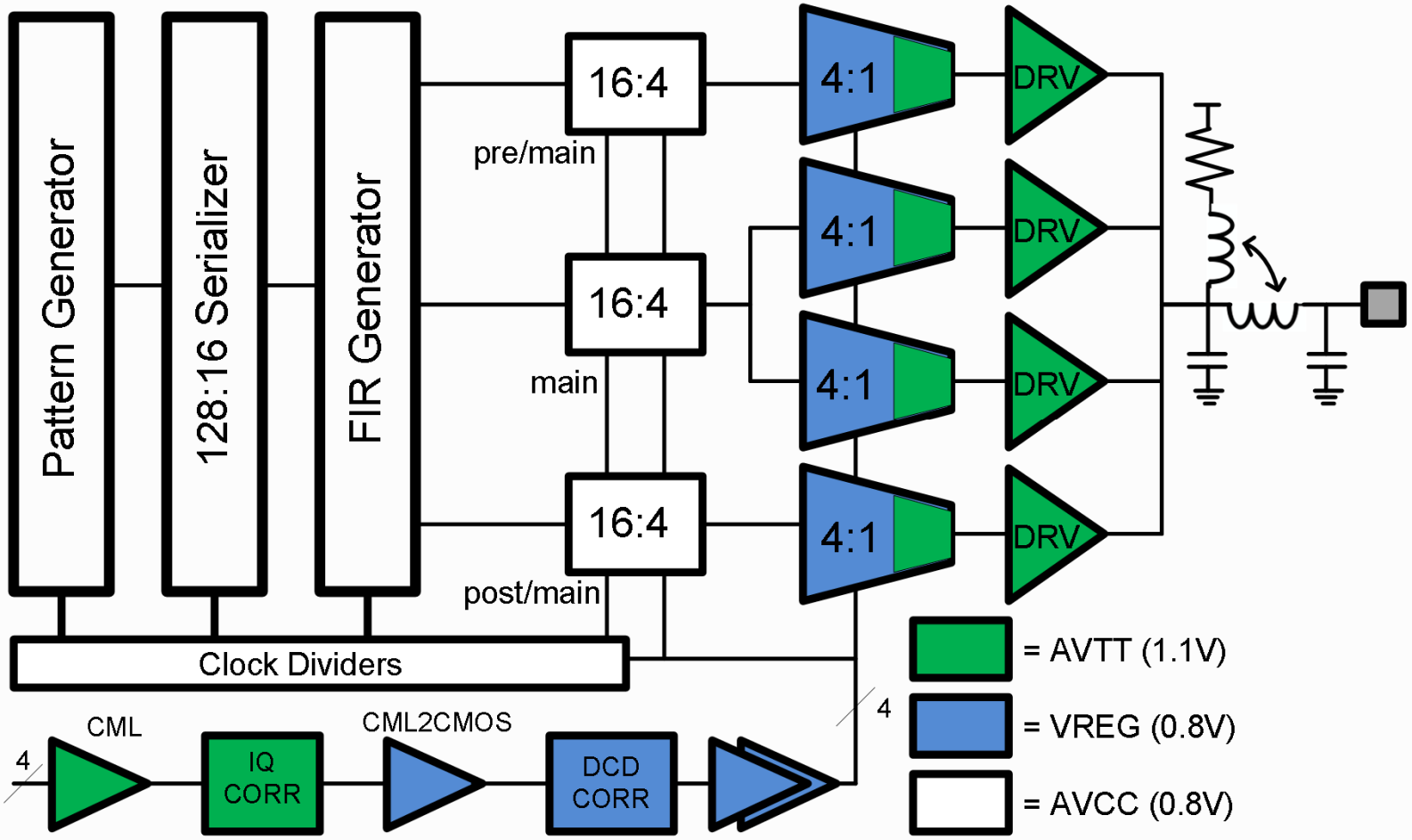
- Up and coming proposal for electrical interface standard includes 56Gb/s data-rate
  - NRZ signaling feasible for short/medium reach
- This work presents a 40-64 Gb/s NRZ Transmitter in 16nm FinFET CMOS Technology
  - Covers 56Gb/s short/medium reach standard
  - Foundation for future works (~112Gb/s PAM4 expected)
  - Considers FinFET device properties

FinFET Device Properties



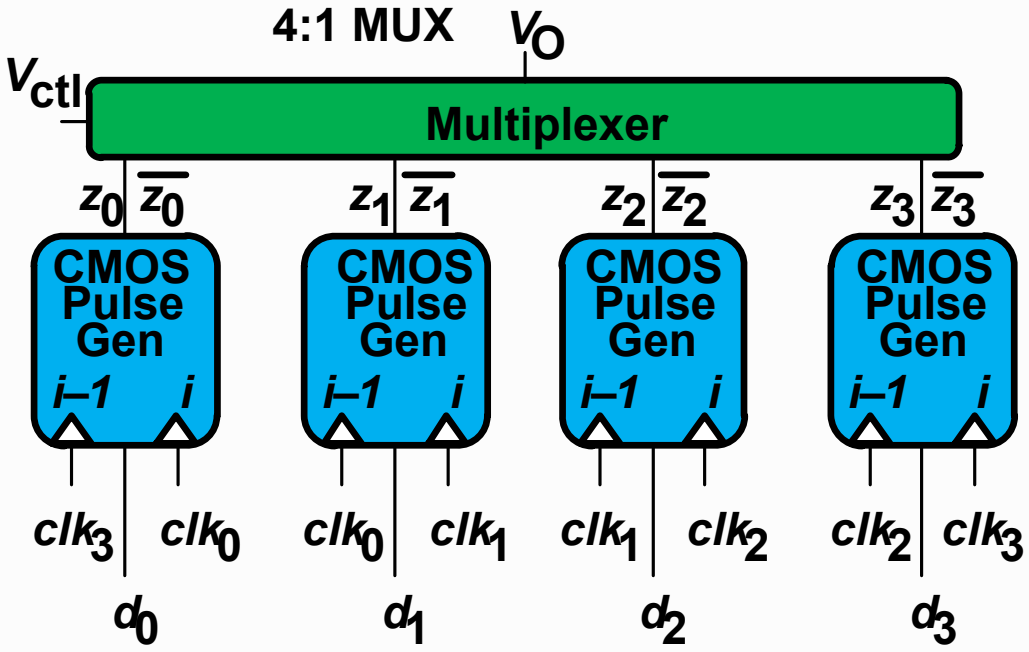
- Advantages
  - Fully depleted body, excellent short-channel control : high mobility, low body effect, low channel leakage, high intrinsic gain
  - Small S/D junction cross-section : low junction capacitance
- Challenges
  - high gate capacitance and resistance
  - high flicker noise
  - steep C-V curve in accumulation region

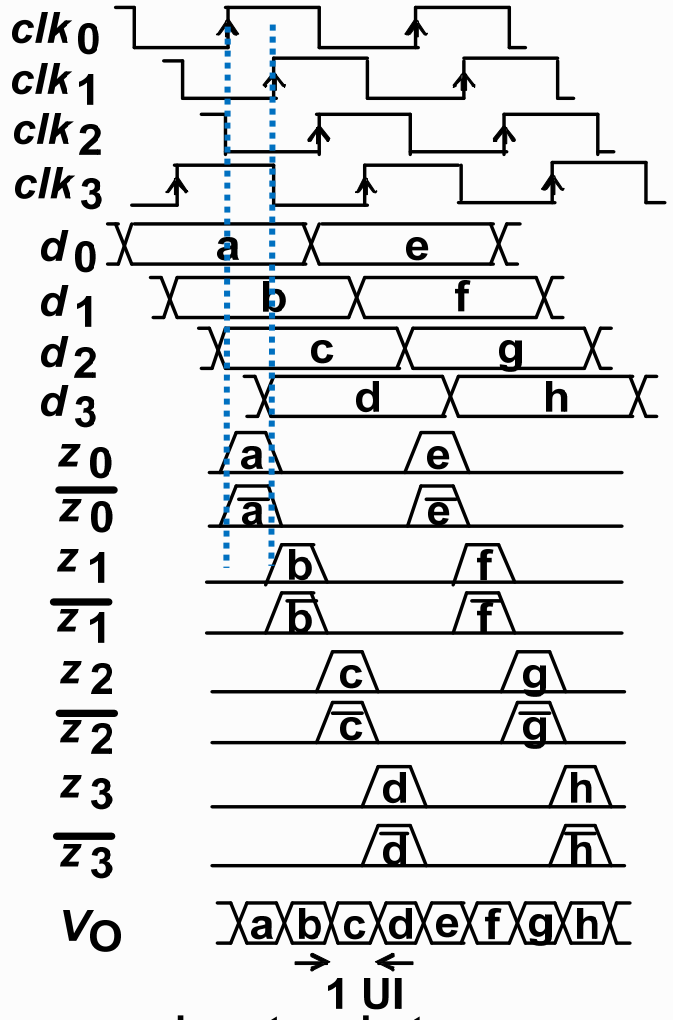
Transmitter Overview



- Quad-rate Architecture [Hafez, ISSCC ’13]
- 3-tap FIR, Regulated Supply Front-End

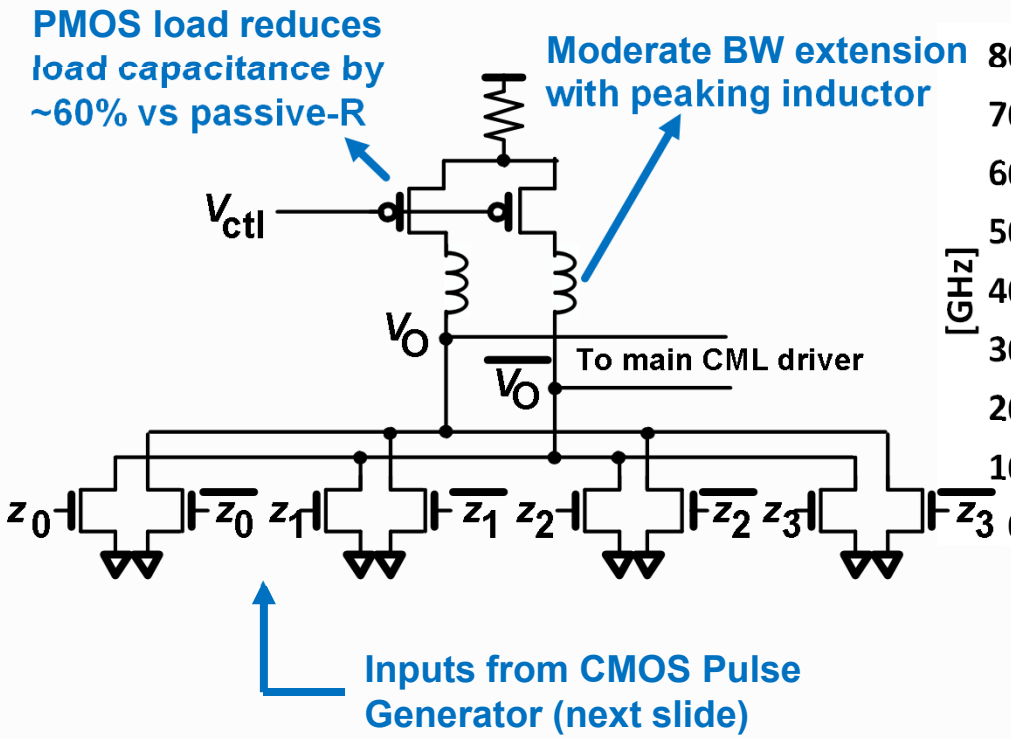
Transmitter Front-End 4:1 MUX

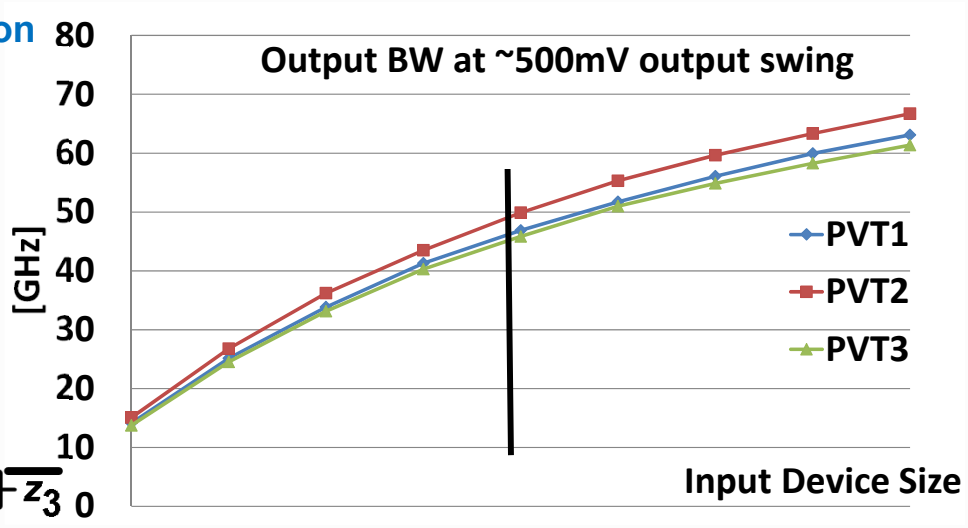




- Stage 1 : Generate 1-UI pulses from quad-rate data
- Stage 2 : Multiplex 1-UI pulses into serial bit-stream

Tail-less Multiplexer



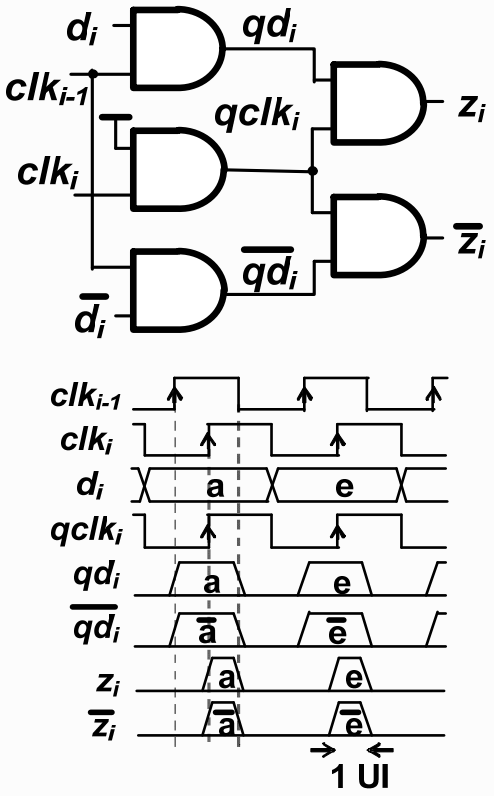


- Input devices sized to get ~45GHz BW

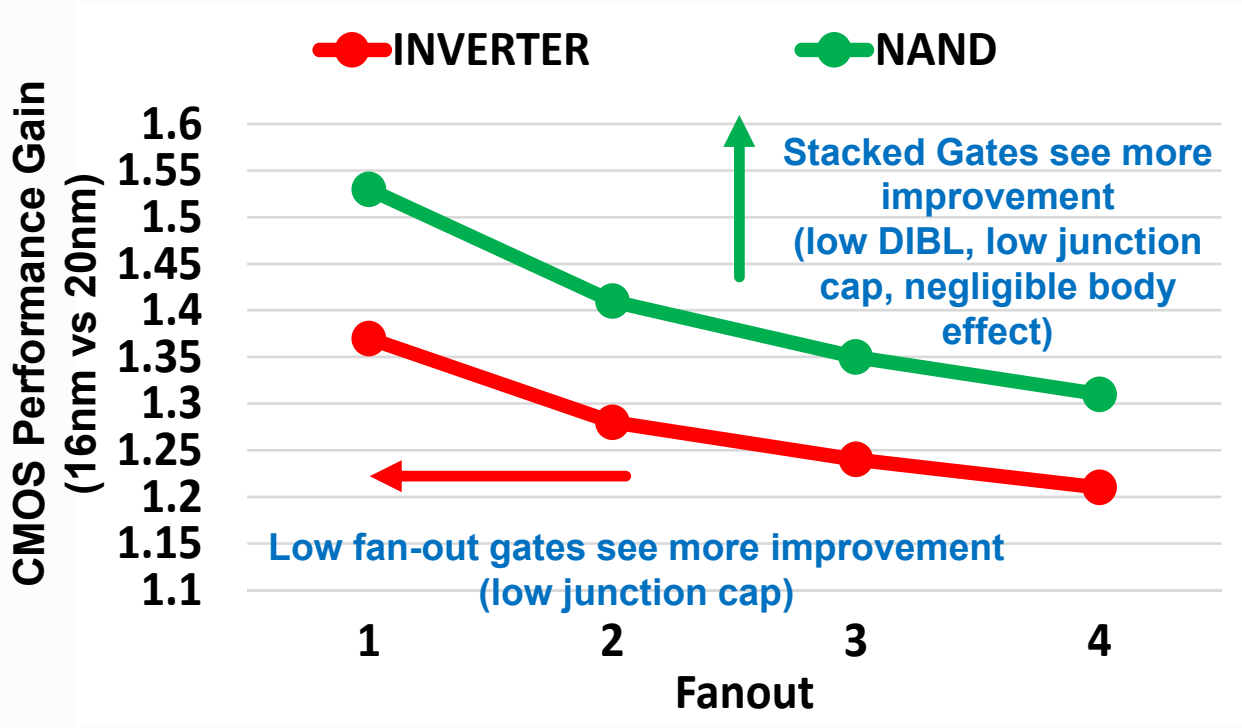
- ~500mV output swing required to fully steer the main CML driver
- Use simple structure to get high-swing and high bandwidth
  - Data qualification done in the previous stage
- Tail-less structure allows smaller input devices
- Common-mode ripple suppressed by main-driver CML stage

CMOS Pulse Generators

Data-qualification in static CMOS

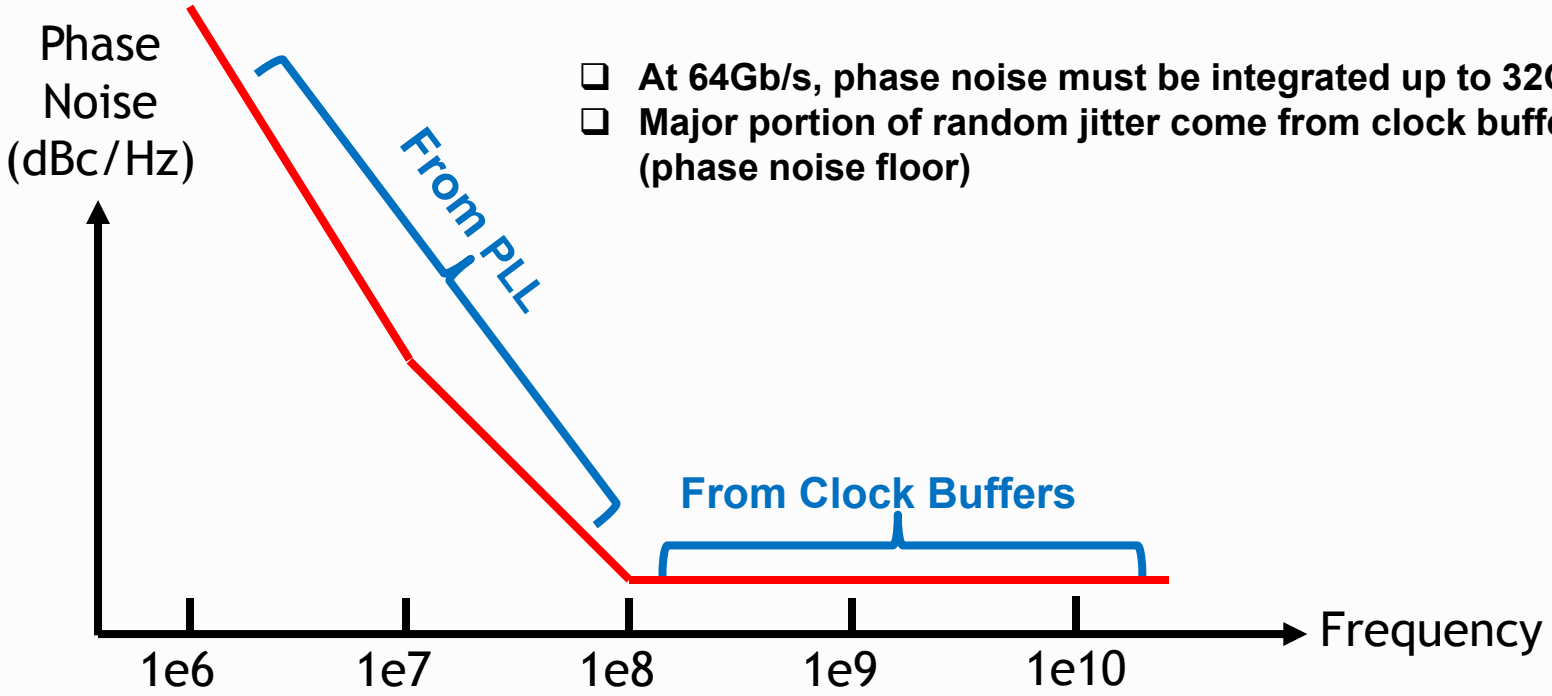


Performance Gain of Logic Gates (16nm vs 20nm)



- Low fan-out, stacked logic gates (e.g. NAND, NOR) see significant performance improvement in FinFET
  - Good-fit for data-qualification portion of 4:1 MUX

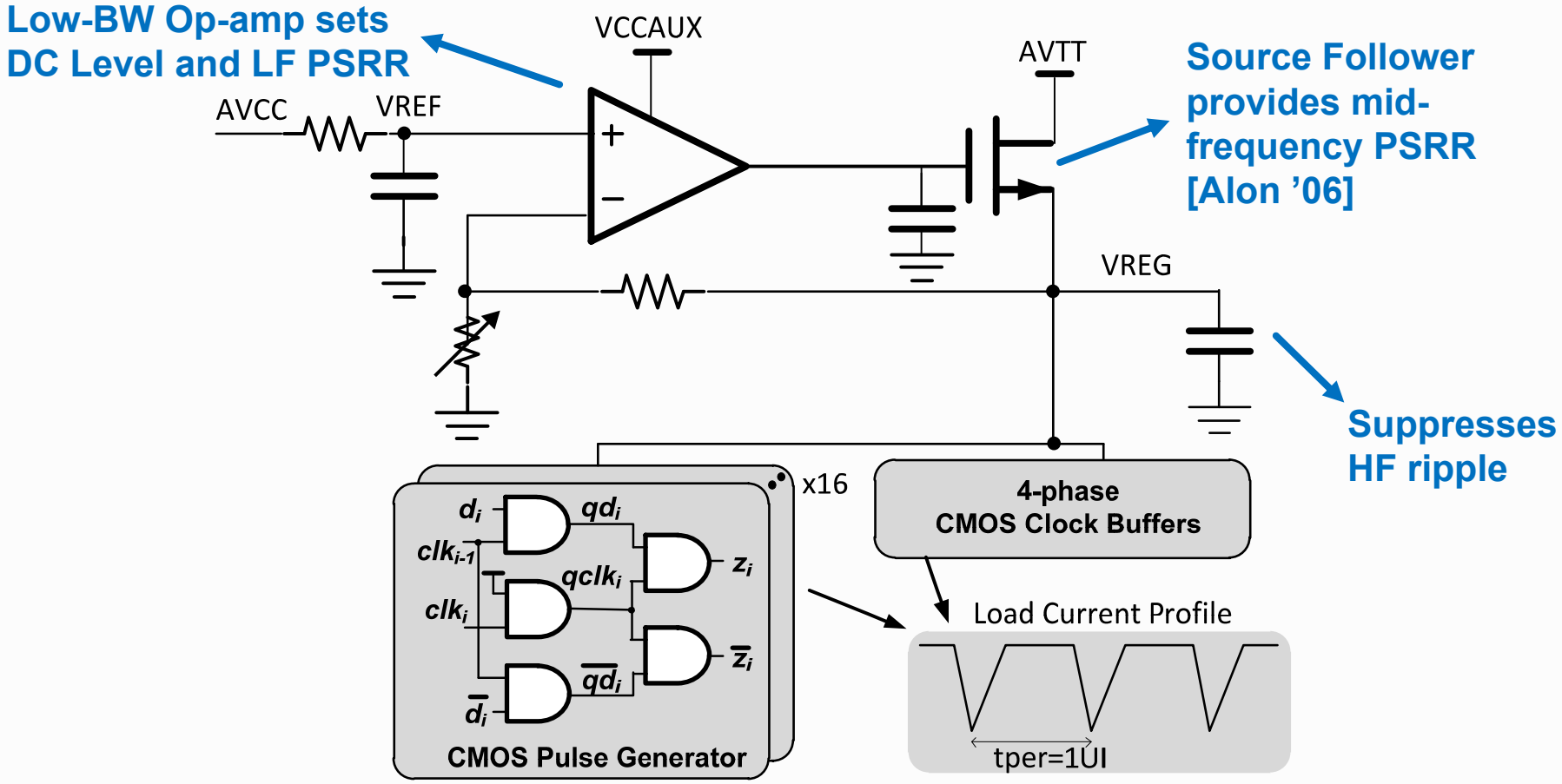
Transmitter Clocking



- ❑ **At 64Gb/s, phase noise must be integrated up to 32GHz**
- ❑ **Major portion of random jitter come from clock buffers (phase noise floor)**

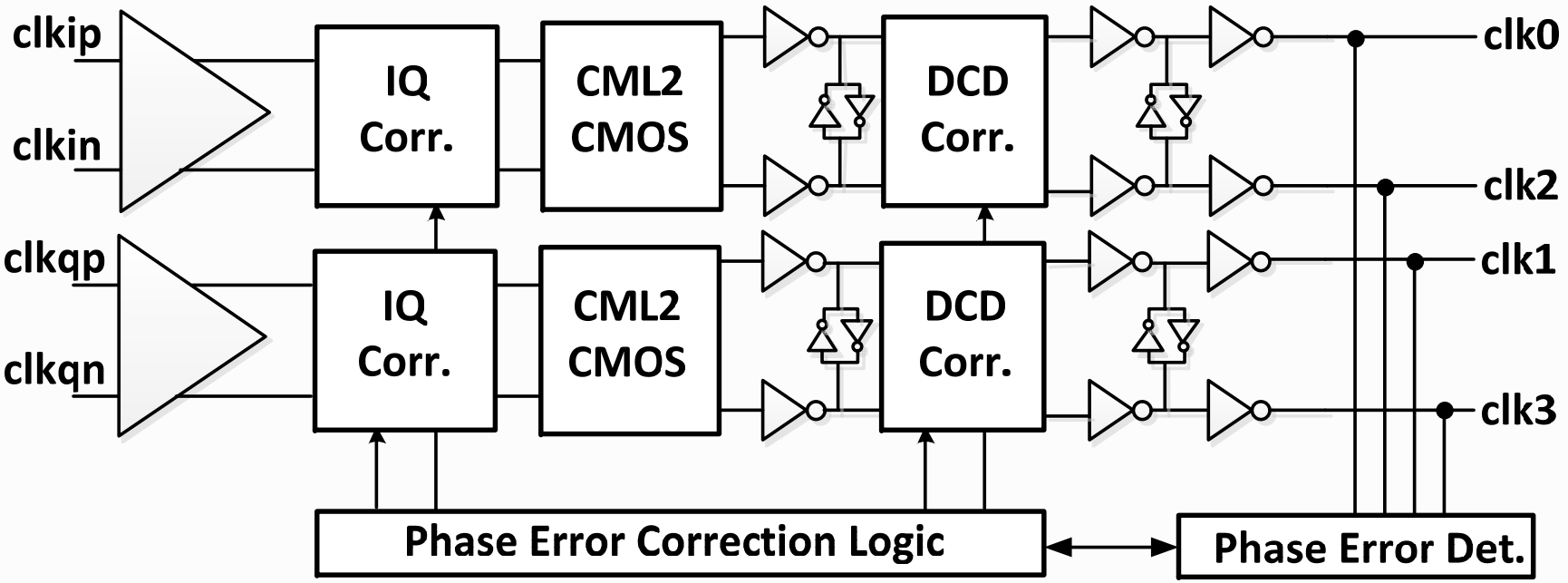
- Clock Buffers using Regulated CMOS
  - Minimize Random Jitter (fast edge Rate)
  - Reduces Supply-Noise-Induced Jitter
- Phase Error Correction
  - Minimize High-Frequency Periodic Jitter

Supply Regulation



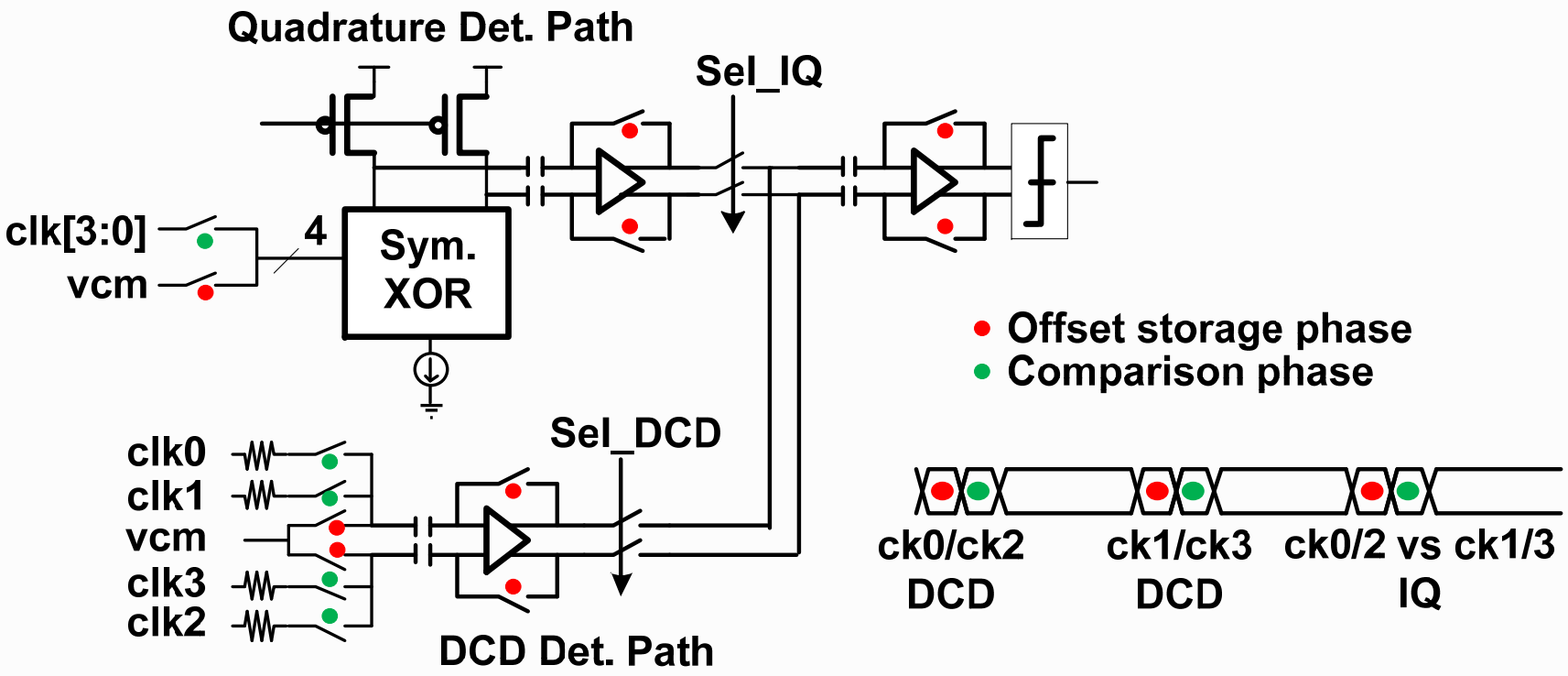
- Load Current Profile : periodic droop at line rate
- Periodic ripple at line-rate doesn't impact jitter
- Residual HF ripple effectively suppressed by decoupling cap

Phase Error Correction



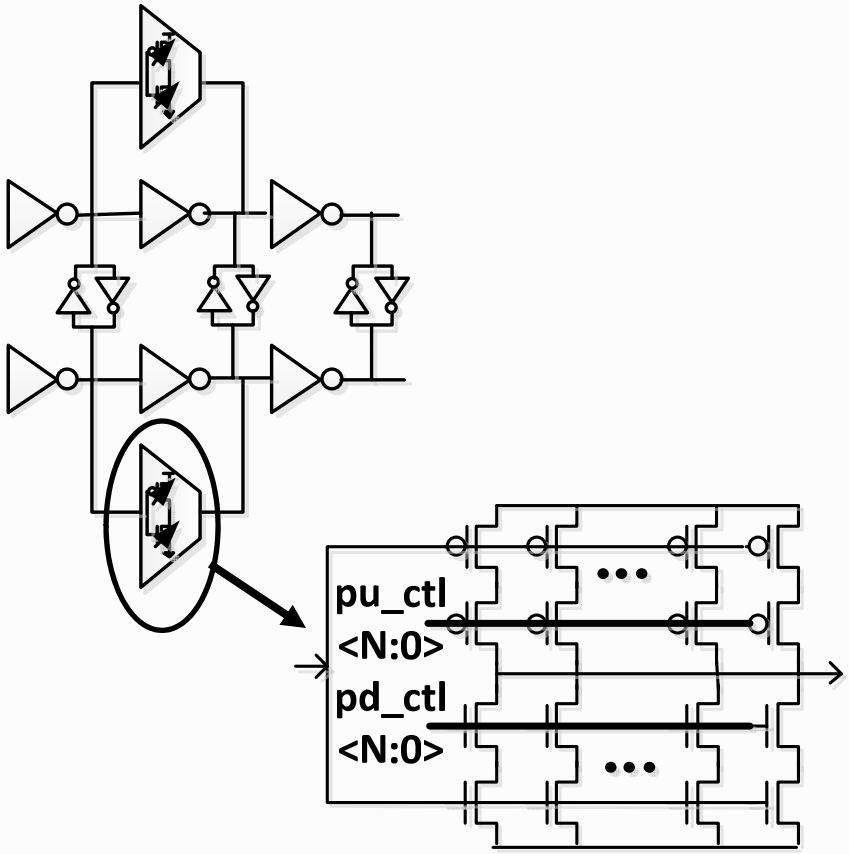
- Step 1: Correct 180^{o} phase between ck0-ck2 and between ck1-ck3
  - Cross-coupled inverters force clk0-clk2 to be differential -> simple DCD detection can be used
- Step 2: Correct 90^{o} phase between clk0/clk2 pair and clk1/clk3 pair

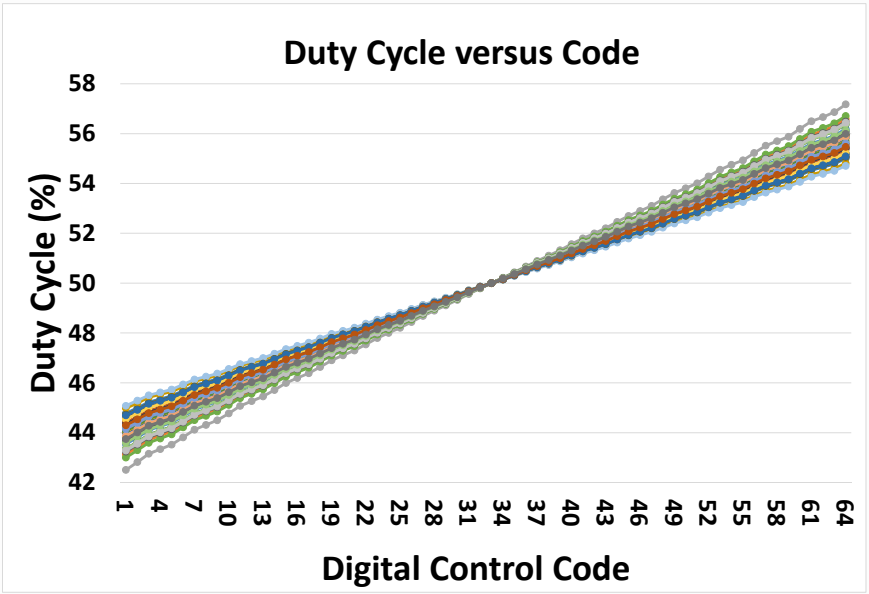
Phase Error Detection



- Time-multiplex DCD and Quadrature Error detection
- Auto-zero comparator performs well in FinFET
  - High intrinsic gain, low channel leakage

Duty Cycle Correction

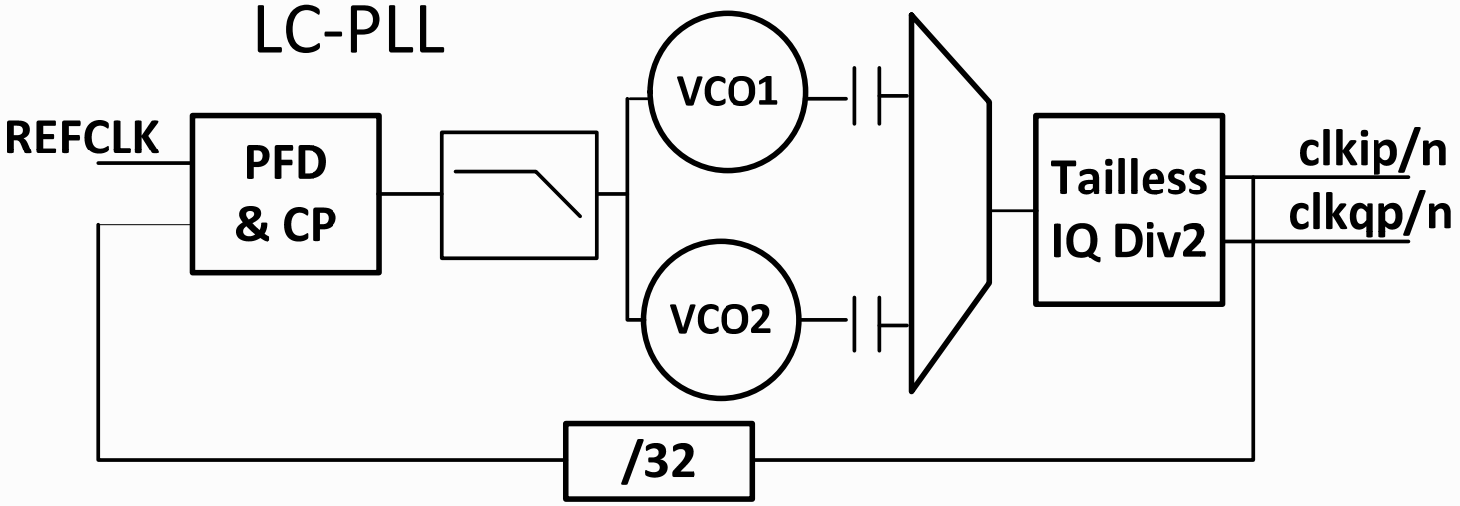




- Correction Range > 4%

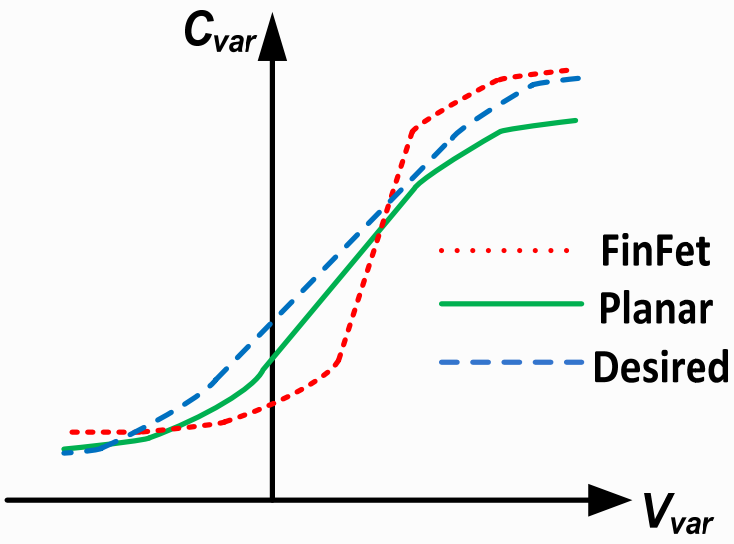
- Digital DCD Correction in CMOS
  - Controls rise/fall time by turning on/off NMOS and PMOS segments
- IQ Correction in CML [Upadhyaya ISSCC'14]

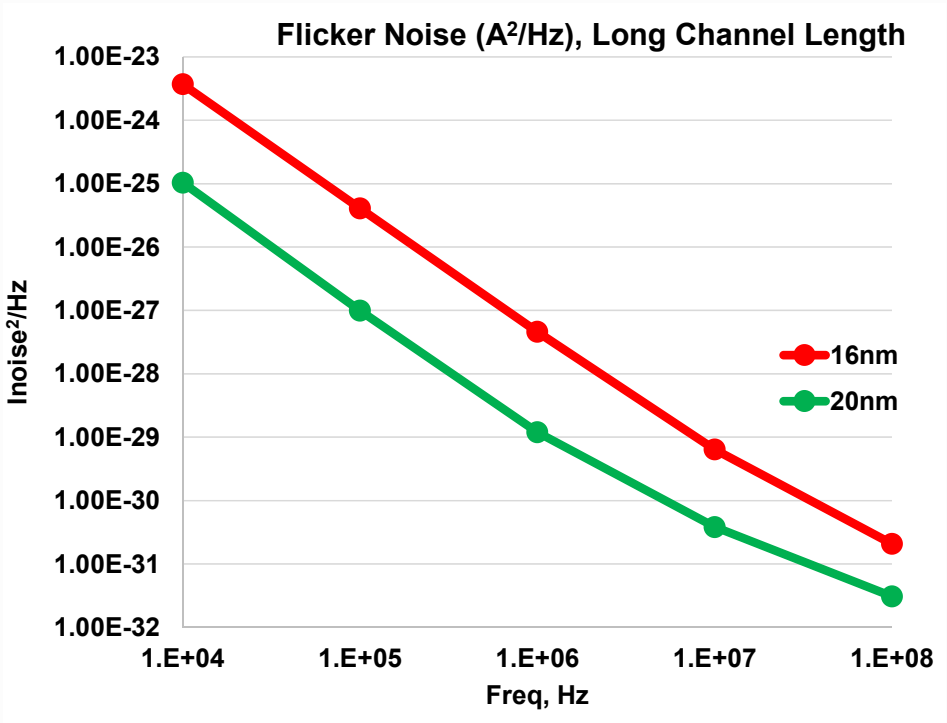
Phase Locked Loop



- Using half-rate VCOs (20GHz to 32GHz)
  - Two VCOs used to cover the range
- Tailless IQ-Div2 structure is used to enable higher speed

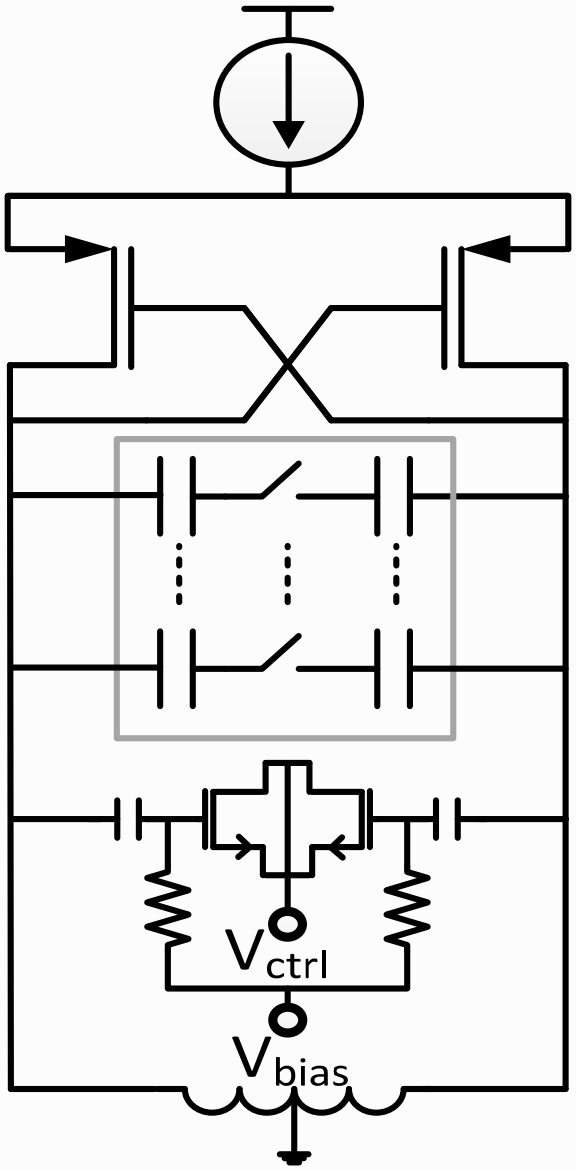
VCO Design Challenges





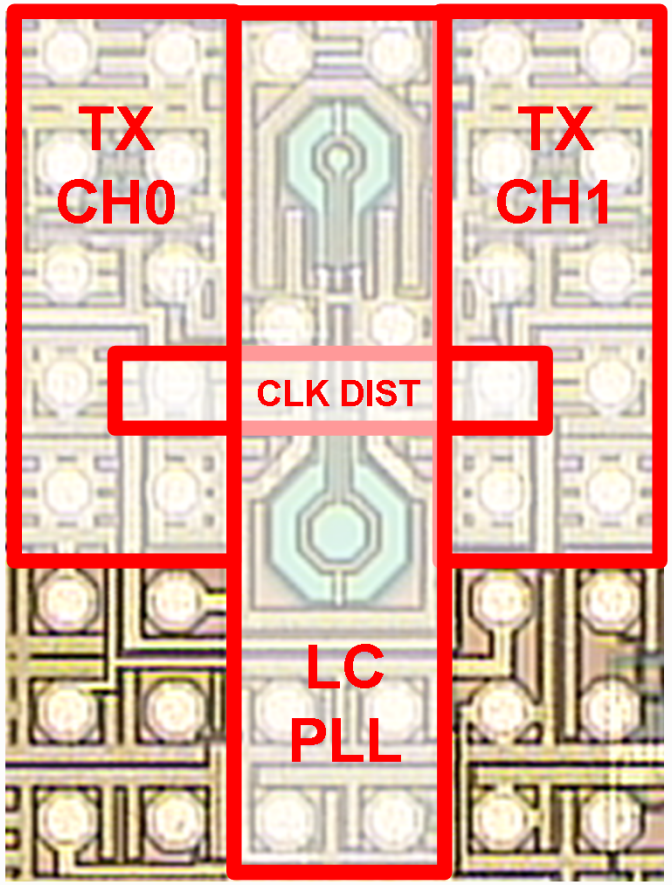
- Varactor CV curve in FinFET is steeper than planar
- Flicker Noise is also higher than planar

LC Tank



- Use large swing (>800mV diff-pp) to linearize Varactor CV curve
- Use GND common-mode to mitigate impact of current-source flicker noise
  - PMOS gm-cell, P/N Beta Ratio ~1
- Metal capacitor banks for coarse tuning
- Varactor for continuous fine loop

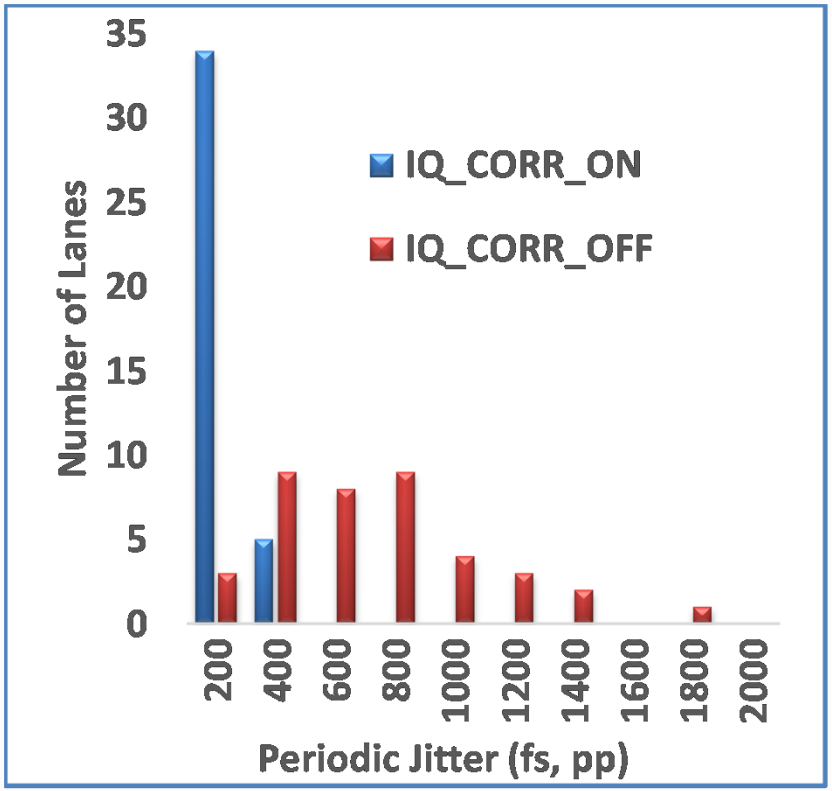
Die Micrograph



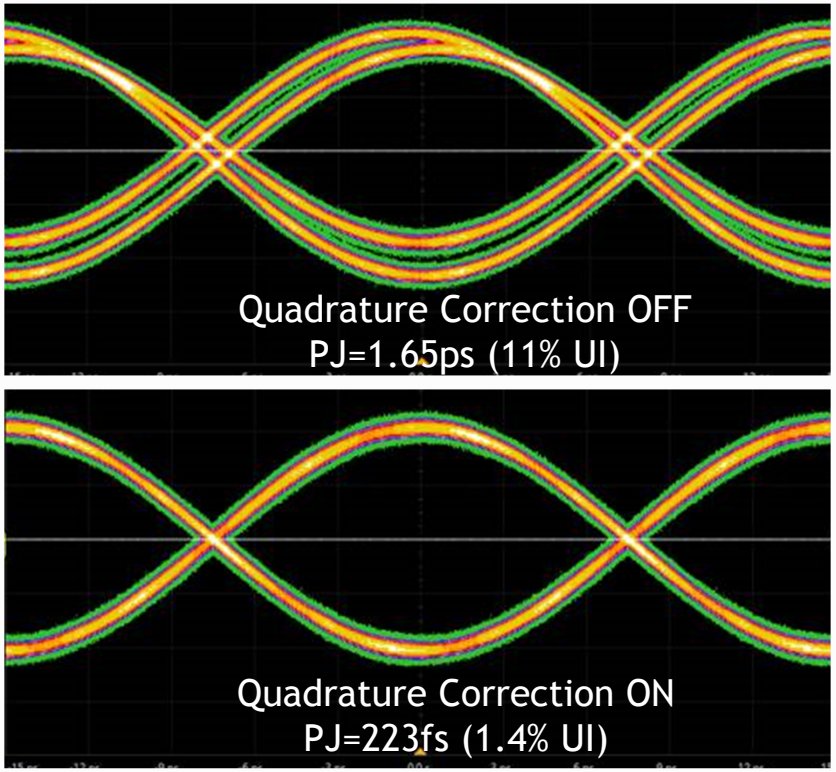
- Fabricated two TX channels
- One common PLL for both channels

Measurement Results (I/Q Correction)

High Frequency PJ Distribution
(20 dies, 40 lanes, 1 wafer)

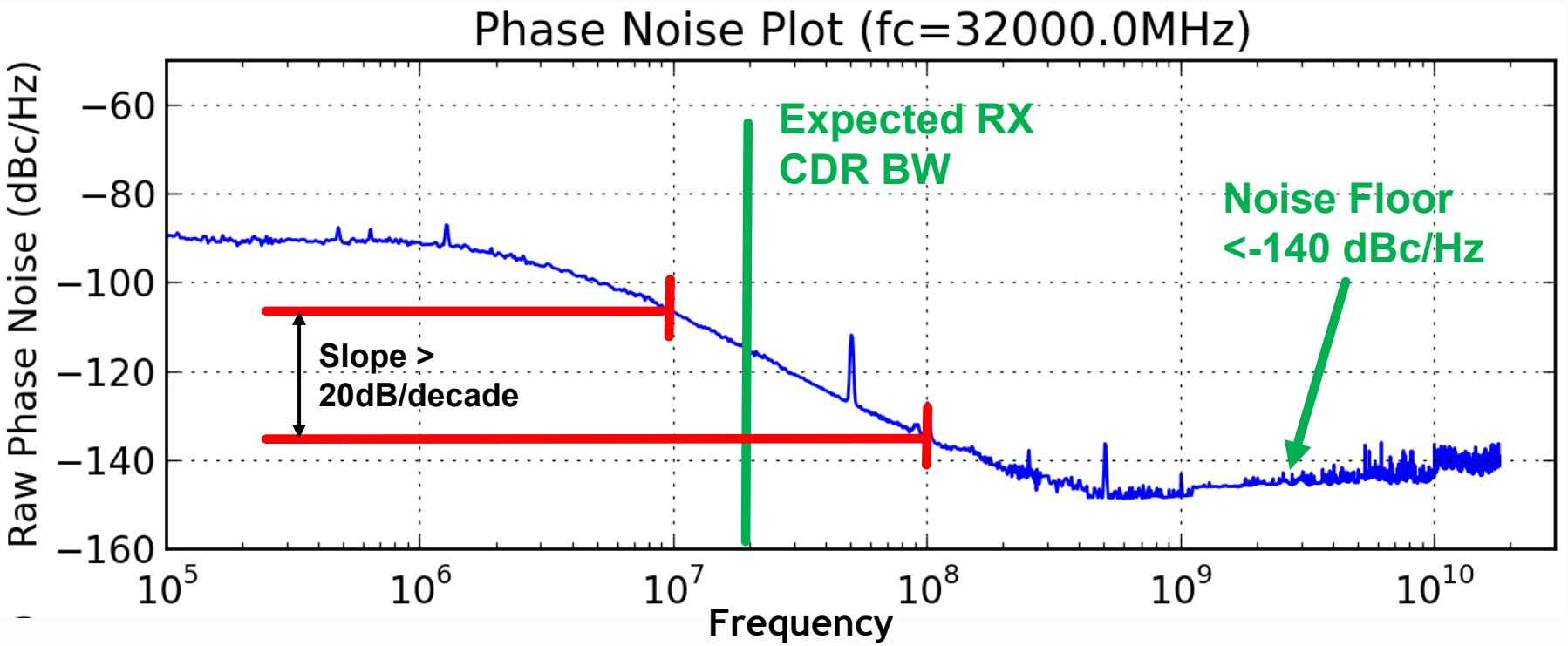


Clock Pattern, 64Gb/s



- Significant high-frequency periodic jitter from phase error due to local mismatches
- Phase Error Correction tightens high-frequency PJ distribution

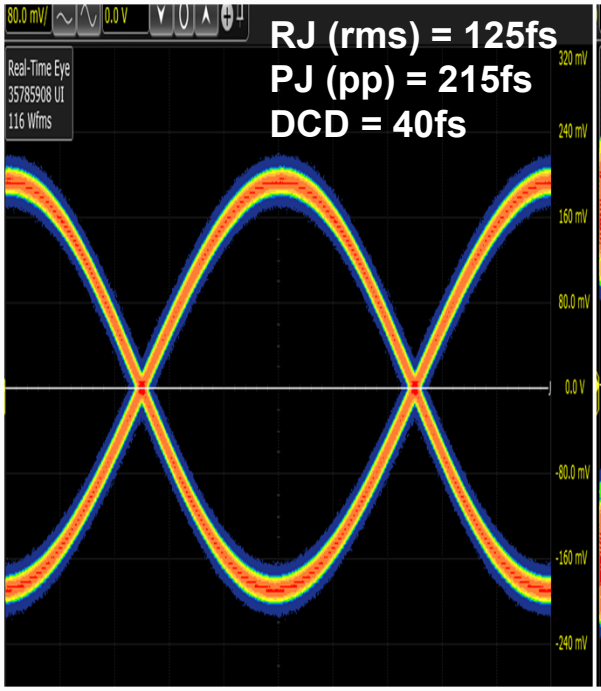
Phase Noise Measurement



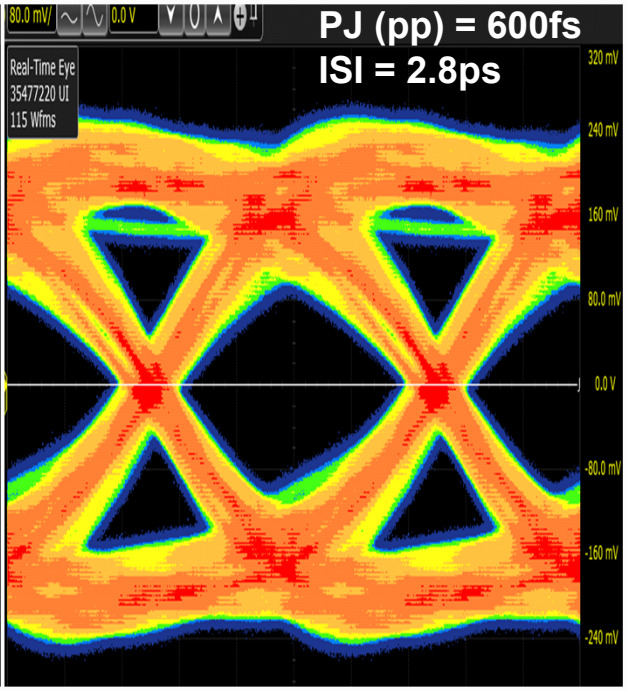
- Low phase noise floor from the use of CMOS clock buffers
- No significant spurs from supply noise
- Flicker noise corner > 10MHz, but phase noise level is low
  - Expect CDR filter to suppress it further

Time Domain Measurement (64Gb/s)

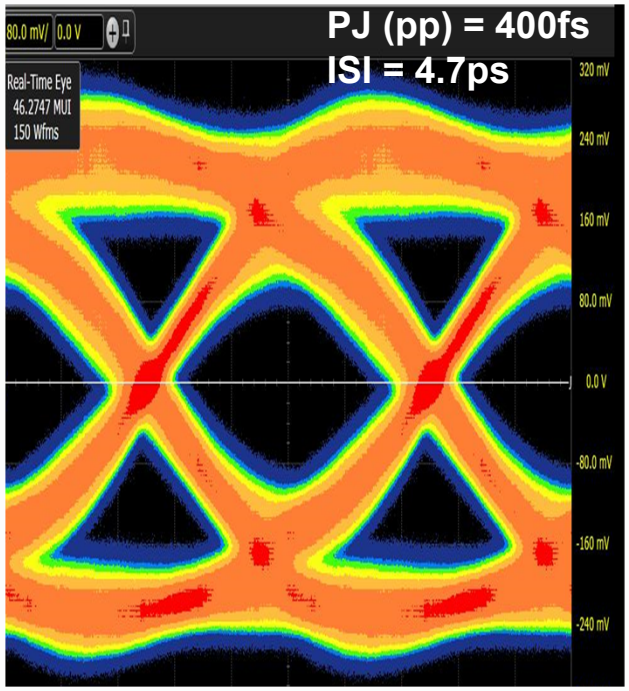
Clock Pattern



PRBS7

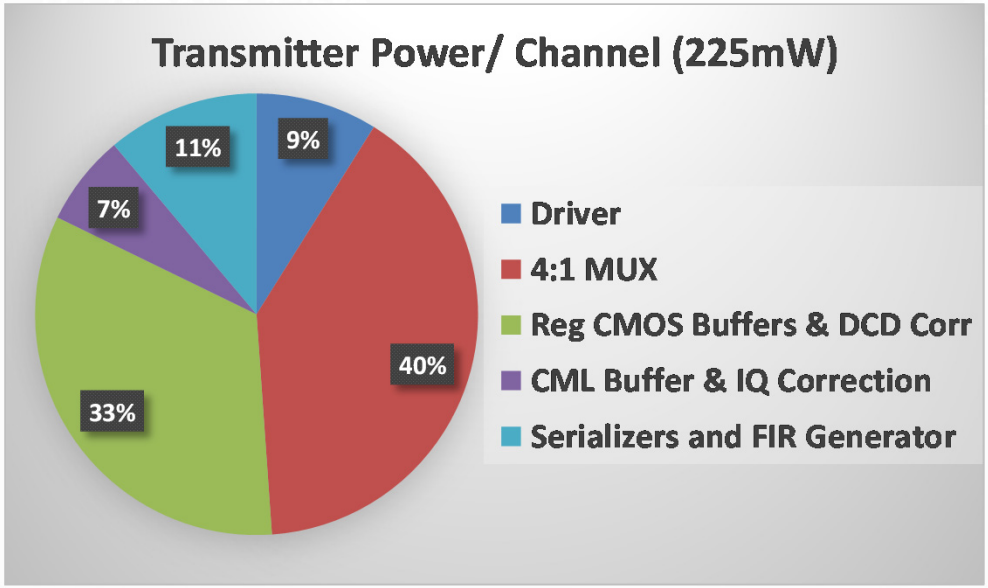


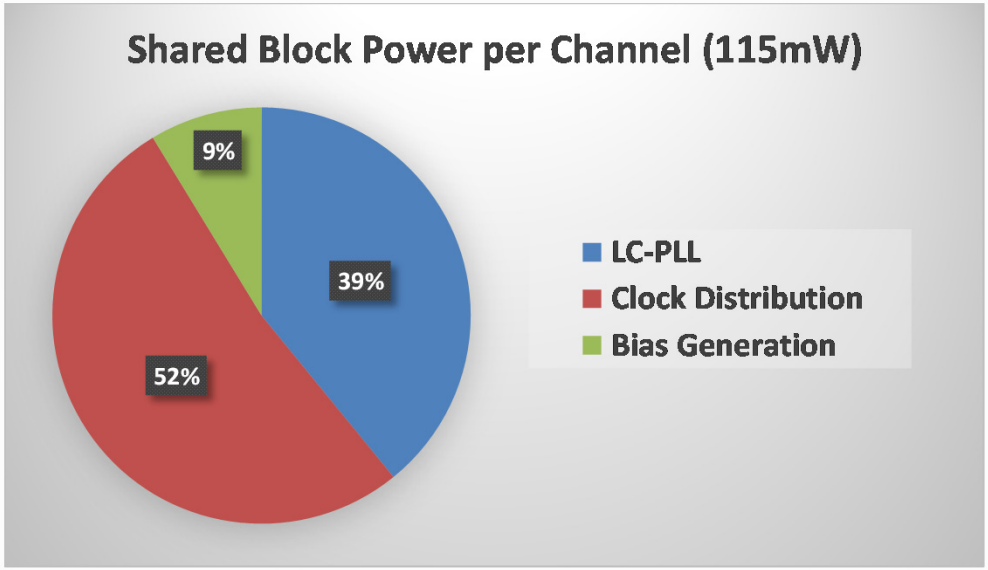
PRBS15



- Measured using Keysight DSA-X96204Q 160GS/s real time scope
- Channel :
  - Channel : 20mm package trace, 1.5” PCB trace, Samtec Bullseye connector, 6” Samtec Bullseye cable, 12” Huber-Suhner cable, and 50GHz DC-blocking capacitors (~6dB total loss)

Power Breakdown at 64Gb/s





Performance Summary

	This work	[Chen CICC'12]	[Jiang ISSCC'14]
Technology	16nm FinFET	65nm CMOS	65nm CMOS
Data-rate	40-64 Gb/s	50-64.5 Gb/s	60Gb/s
FFE	3-tap	4-tap	None
Area (TX Only)	0.32mm2 (C4 array limited)	0.35mm2	2.1mm2
Power (TX) per channel	225mW @ 64Gb/s	199mW @64Gb/s	450mW @60Gb/s
Power (PLL+Clock Distribution) per channel	115mW @ 64Gb/s	N/A	
TX Amplitude (No EQ, diff-pp)	800mV	850mV	500mV
Wide-band TX Jitter (Clock Pattern)	RJ-rms=150fs PJ-pp=200fs DCD=30fs	Not reported	Not reported (narrow-band rms=461fs from 1kHz to 20MHz)
TX Jitter (PRBS)	PJ=600fs ISI=2.8ps	Not reported	Not reported

Conclusion

- A 40-64Gb/s 3-tap NRZ Transmitter with quad-rate architecture and regulated CMOS clocking is designed in 16nm FinFET
- The transmitter design takes advantage of good channel control and small junction capacitances in 16nm FinFET devices
  - Allows the use of static CMOS in 4:1 MUX data qualification
  - Increases the performance of supply regulator and phase error detector
- Challenges in LC-VCO design is overcome using higher swing and ground common-mode
- The transmitter achieves targeted jitter performance

Acknowledgement

- The authors thank Xilinx Serdes team for their contributions in circuit design, chip bring-up, and measurements